RACAL

RA-6790/GM

hf receiver

500khz-30Mhz

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RACAL RA6790 INSTRUCTIONS

1. Turn on POWER 2. Establish LOCAL control via LOCAL/REMOTE button 3. INITIALIZATION: (a) Press and hold LOCK button, then AM button (on left keypad,) releasing simultaneously; (b) Word 'REMOTE' will appear, then the frequency and BFO digits will rapidly scan through their ranges-accompanied by various changing sounds and tones; changing modes and levels will follow also; (c) If the sequence stops and displays a 2 digit byte number, the self-check has detected an error condition.

EXTERNAL SPEAKER CONNECTIONS

The LOUDSPEAKER OUT connections for the RACAL RA6790 are found on J3 (DB25F) on the rear panel. Use a DB25P with the connections as listed below:

LOUDSPEAKER OUT: pin 18 SIGNAL GND: pin 6 CHASSIS GND: pins 7, 8, & 9

TITLE: RACAL RA6790 INSTRUCTIONS STARTUP / INITIALIZATION / TUNING with EXT. SPEAKER CONNECTIONS		PAGE NR: 1 of 1 CONNECTIVE COUNT: n/a VERSION: 1.0
FILENAME: RACAL.SKD	SECTION: HR\LOGOS	DATE: 95 10 28
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RACAL
COMMUNICATIONS INC.

TECHNICAL MANUAL
FOR
RA6790/GM
HF RECEIVER
RCI 84249
(R-2174)
(R-2174A)

#9767

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CONFIGURATION NOTICE: This document contains technical information pertaining to the basic RA6790/GM HF Receiver and to the modified RA6790/GM HF Receiver, resulting from the addition of an AGC level return software modification. That information pertaining to the basic RA6790/GM HF Receiver is provided in Sections I through VII of this document whereas, information pertaining to the modified RA6790/GM HF Receiver is provided by difference data in Section VIII of this document.

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HF RECEIVER
RCI 84249
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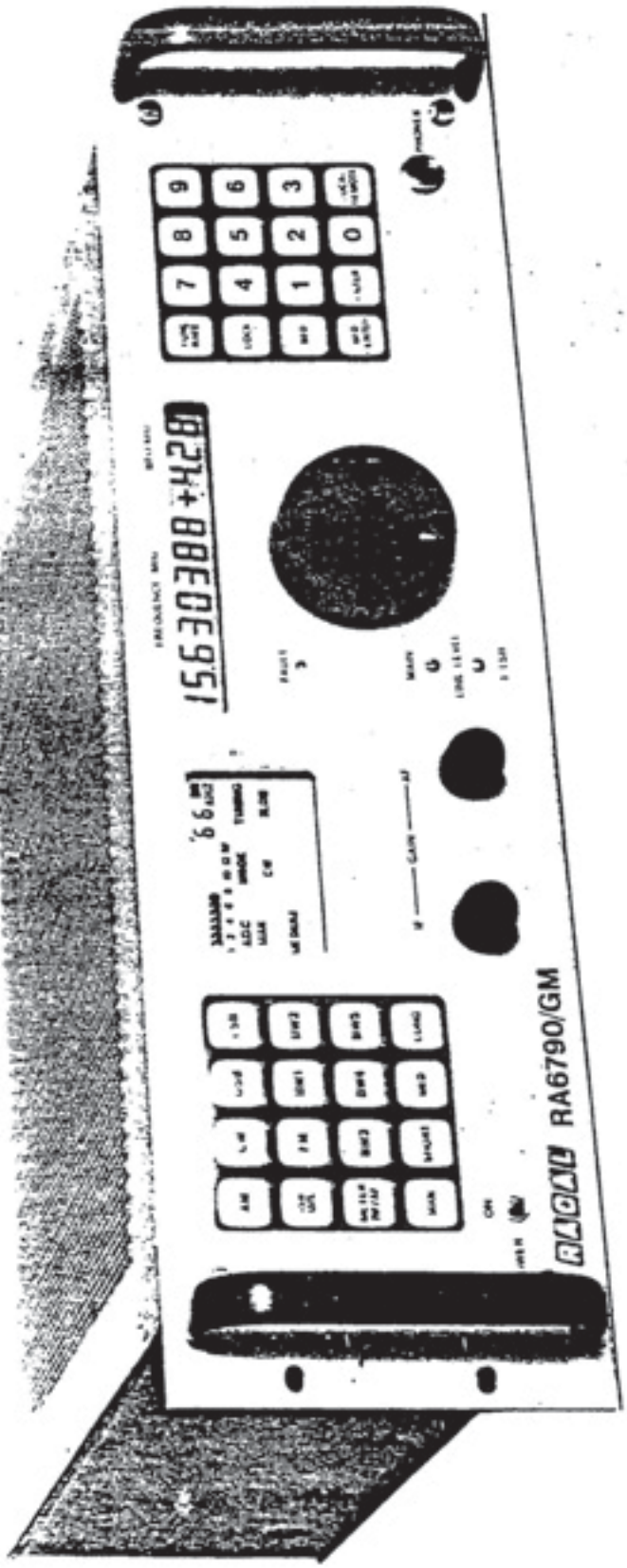

Figure 1-1. Overall View, RA6790/GM HF Receiver

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SECTION I
GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The RA6790/GM HF Receiver, shown in Figure 1-1, is a fully synthesized, microcomputer-based, tunable, solid-state receiver designed to provide reception capabilities for CW(A1), AM(A3), LSB/USB (A3J), FM(F3) and ISB (A3B-Optional), emissions over the frequency range of 0.5 MHz to 30 MHz. Frequency tuning is accomplished by either keyboard entry (numerical keypad) or single knob control for continuous tuning with selectable rates, FAST (1000 Hz), SLOW (30 Hz), FINE (1 Hz) increments and BFO continuous in 10 Hz increments. Front panel indication of frequency data are presented as 8 LCD (Liquid Crystal Display) digits of tuned frequency and 3 digits and sign readout of BFO data relative to IF Center ±8.0 kHz. Other front panel displays are: RF Meter, AF Meter, Bandwidth, AGC, Mode, Remote and Fault indication (LED). Additionally, provision is made on the front panel, selectable by use of the RF Gain Control, to manually control the AGC threshold anywhere within the range of 110 dB above the preset AGC threshold level.

Full remote control (optional) of all Receiver parameters is available by either; (1) serial asynchronous, ASCII character-oriented with strap selectable baud rate of 50 baud to 19.2 kilobaud, selectable MIL-STD-188C or EIA Standard RS-232-C/RS-422/RS-423 compatible, 2-byte-serial, (2) byte-serial bit parallel IEEE standard 488C-1978 compatible or (3) other user specified interface format.

Built-In Test Equipment (BITE) is provided in the Receiver circuitry to find, test and report operational status to the lowest replaceable unit (LRU) with both local and remote notification.

The internal frequency tuning circuitry of the Receiver includes a single loop digital 1st LO Synthesizer, phase lock loop 2nd LO and BFO Synthesizers, which in combination determine tuned frequency to a resolution of 1 Hz. The synthesized BFO tunes ±8 kHz in 10 Hz increments with a pushbutton selectable parameter for immediate zero reference.

The Receiver is designed to operate with up to seven IF filters, using slots provided on the Main IF/AF circuit card assembly. Unless otherwise specified, the Receiver is factory equipped with six mechanical filters and one bypass link to provide seven selectable bandwidths. Audio output of the Receiver is either through a PHONES jack on the front panel or through an AF OUT connector on the rear panel. The PHONES jack provides a nominal 10 milliwatts into 600 ohms and is adjustable through the AF GAIN control on the front panel. The AF OUT connector provides a nominal 1 milliwatt 600 ohm balanced line output and an output of nominally 1 Watt in 8 ohms, suitable for an 8 ohm speaker.

Rear panel features include BNC connectors for providing the Receiver second IF 455 kHz output, supplying or receiving external/internal reference signals used in conjunction with a slide switch, S2. A 25-pin D-type connector provides audio, AGC and fault status outputs while an N-type connector provides RF input from an external antenna. An optional remote control interface connector, either round 26 pin (188C/232C/422/ 423) or elongated 24 pin (IEEE-488), is provided when specified. A standard 3 prong male connector for connection of an ac line cord completes the rear panel assembly.

Input signals from the antenna are connected to a low pass filter which rejects signals above 30 MHz. The output of this filter is then coupled to a mixer stage where the RF signal is mixed with the synthesized local oscillator signal. The frequency of the local oscillator can be varied

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from 40.955 to 70.455 MHz. This signal is brought through a filter and AGC controlled amplifier stages to the second mixer.

The 40.455 MHz first IF is combined with the fixed 40 MHz output from the second oscillator synthesizer to produce a 455 kHz second IF. After amplification, this second IF is routed to the plug-in 455 kHz filters which provides the main Receiver selectivity.

A second AGC-controlled amplifier follows before demodulation takes place. In the SSB/CW/AM modes, a product synchronous detector is used. In the CW mode, the BFO synthesizer may be varied ±8 kHz (above or below the 455 kHz center frequency) through front panel controls. For FM reception, the 455 kHz second IF is input to a limiting amplifier and subsequently to a separate FM detector. All three outputs from the synthesizers are referenced to an internal 5 MHz standard frequency source, or to an external reference of 1 MHz. The demodulated signal is fed through an audio crosspoint switch to separate AF amplifiers which provide outputs for a 600 ohm line, a headphone jack, and an external loudspeaker.

For ISB operation, the optional ISB board provides the LSB signal path, while the main IF/AF board provides the USB signal path. The LSB component of the 455 kHz second IF is processed through similar circuitry with the common BFO synthesizer providing the reinserted carrier for demodulation. A separate audio amplifier provides a 600 ohm line output.

All command signals, whether from the front panel controls or from an extended or remote operating position, are processed by the microcomputer assembly. Two separate buses carry control data and address information to and from the microcomputer control assembly to the synthesizers for frequency selection, and to the appropriate switching circuits controlling the different operating modes.

1.2 MECHANICAL CHARACTERISTICS

The RA6790/GM Receiver mounts in a standard 19-inch (48.3 cm) equipment rack, and occupies 5.25 inches (13.33 cm) of vertical space, 19 inches (48.3 cm) wide, 18.5 inches (47 cm) deep and weighs 30 pounds (13.5 kg).

A rigid, die-cast full width chassis is used as the base for the main frame of the Receiver. Mounted within compartments on the underside of this chassis are the mixer boards and the frequency generation system. The input low pass filter, main IF/AF, optional ISB IF/AF and power supply modules are located on the top surfaces of the die-cast chassis while the control and digital I/O modules are attached on the Receiver main frame. All modules are accessible for maintenance and can be removed or replaced using simple hand tools without the use of a soldering iron.

Manual controls and indicators for operation and monitoring of the Receiver are contained on the front panel while input/output jacks and connectors are provided on the rear panel. A PHONES jack, for audio connection to optional headphones, is contained on the front panel for convenient access. A primary power fuse is accessible from the rear panel.

1.3 EQUIPMENT SUPPLIED

The equipment supplied consists of the following:

1. RA6790/GM HF Receiver
2. W18, Primary Power Input Cable
3. Connector, Mating for J3

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4. Six Mechanical Filters.
Unless otherwise specified the filters shall conform to Racal part numbers 07883-1 thru 07883-6. Refer to Paragraph 1.4, Item #2 below for details.

1.4 OPTIONAL EQUIPMENT

The following optional equipment is available for use with the RACAL RA6790/GM HF Receiver. Additional information regarding these and other options should be made through your RACAL representative or directly to RACAL Communications, Inc., Rockville, Maryland, USA.

1. Independent Sideband Module (ISB, A5);

2. Selectable IF Bandwidth Mechanical Filters:

	Bandwidth	Description	Shape Factor 3 dB: 60 dB	Racal Number
1.	0.3 kHz	Symmetrical BPF	1:6.7	07883-1
2.	1.0 kHz	Symmetrical BPF	1:4.5	07883-2
3.	3.2 kHz	Symmetrical BPF	1:2.7	07883-3
4.	4.0 kHz	Symmetrical BPF	1:2.5	3600001
5.	5.0 kHz	Symmetrical BPF	1:2.5	3600002
6.	6.0 kHz	Symmetrical BPF	1:2.3	07883-4
7.	450 Hz to 3000 Hz	ISB/USB BPF	1:1.92	07883-5
8.	450 Hz to 3000 Hz	ISB/LSB BPF	1:1.92	07883-6
9.	350 Hz to 2700 Hz	USB BPF	1:1.66	08669
10.	300 Hz to 2200 Hz	USB BPF	1:1.97	08771

Note that input and output matching capacitors are required with mechanical filters only, contained on assembly A4.

3. Selectable IF Bandwidth Crystal Filters:

The Receiver may be operated with one to seven different crystal bandwidth filters. There are currently a total of 23 different filters available; however, depending on Receiver configuration, some filters are mandatory. (Refer to the Installation Section of this manual for definition of IF Bandwidth Filter Installation.)

Bandwidth	Description	Shape Factor 3 dB: 60 dB	Differential Delay μS	Racal Number
1.0 kHz	Symmetrical BPF	1:6	25	3600003
3.0 kHz	Symmetrical BPF	1:6	13	3600004
6.0 kHz	Symmetrical BPF	1:6	10	3600005
1.0 kHz	Symmetrical BPF	1:2.5	1080	3600006
3.0 kHz	Symmetrical BPF	1:2.5	360	3600007
6.0 kHz	Symmetrical BPF	1:2.5	180	3600008
0.125 kHz	Symmetrical BPF	1:5.33	–	08699
0.4 kHz	Symmetrical BPF	1:6.2	–	08406
1.2 kHz	Symmetrical BPF	1:6	–	08407
6.8 kHz	Symmetrical BPF	1:3.3	–	08408
350 Hz to 3050 Hz	ISB/LSB BPF	1:1.6	800	08409
350 Hz to 3050 Hz	ISB/USB	1:1.6	800	08410
0.4 kHz	Symmetrical BPF	1:2.5	2000	08411

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1.2 kHz	Symmetrical BPF	1:2	1000	08412
3.24 kHz	Symmetrical BPF	1:1.33	1000	08413
6.8 kHz	Symmetrical BPF	1:2	1000	08414
16.0 kHz	Symmetrical BPF	1:2	40	08415
0.5 kHz	Symmetrical BPF	1:6	80	08416
1.0 kHz	Symmetrical BPF	1:6	40	08417
2.0 kHz	Symmetrical BPF	1:6	20	08418
3.0 kHz	Symmetrical BPF	1:6	20	08419
6.0 kHz	Symmetrical BPF	1:6	20	08420
0.075 kHz	Symmetrical BPF	1:6.67	–	08589

4. Remote Control Options (A6A1):

   a. RS-232/RS-422/RS-423 Serial Asynchronous Remote Interface Module
   b. IEEE 488C-1978 Compatible;

5. Improved internal frequency standard ±3 parts 10^{-9};
6. RF Amplifier for greater receiver sensitivity;
7. LF/MF/HF low frequency – 10 kHz to 30 MHz;
8. Broadband IF output.

1.5 REFERENCE DATA

Table 1-1 identifies the technical specifications for the RA6790/GM HF Receiver. The Receiver provides reception capabilities for CW (A1), AM (A3), LSB/USB (A3J), FM (F3) and optionally ISB (A3B) operation. Figure 1-2 depicts the International Reception Mode Codes.

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Figure 1-2. International Reception Mode Codes

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TABLE 1-1. RA6790/GM HF RECEIVER SPECIFICATIONS

Frequency Range	0.5 kHz to 29.999999 MHz
Frequency Resolution	1 Hz increment
Frequency Tuning	By keyboard entry or continuous tuning with selectable rates, FAST (1000 Hz), SLOW (30 Hz), and FINE (1 Hz) increments; BFO continuous in 10 Hz increments.
Frequency Indication	8 digit electronic readout of tuned frequency to 1 Hz; 3 digit and sign readout of BFO relative to IF center ±8.0 kHz.
Frequency Stability	±5 parts in the 10^8 per 10°C temperature increment over the range of 0°C to 50°C using internal 5 MHz reference oscillator. Provision for an external 1, 5 or 10 MHz reference input/output. 0 dBm nominal into 50 Ohms.
Detection Modes	CW/A1 Continuous Wave; CW/A2 Modulated Continuous Wave; USB/LSB (upper/lower sideband) A3A, A3H, A3J, A2A, A2H, A2J; AM/A3 Amplitude Modulation; A4 (Facsimile) ISB/A3B Independent Side Band (optional); FM/F3 Telephony.
Gain Control Modes:	
AGC	Control Range: An increase of 110 dB above AGC threshold will result in a change of output of less than 3 dB. Threshold Range (preset): −113 dBm to −100 dBm Time Constants: Attack: 20 msecs Decay: Short < 30 msecs Medium 200 + 100 msecs Long 3.75 seconds ±1.25 msecs
Manual/Automatic Gain Control	Provision is made on the front panel to select, and by use of the RF Gain Control, to manually control the AGC threshold anywhere within the range of 110 dB above the preset AGC threshold level.
Input Impedance	50 ohm nominal, 2:1 VSWR Type N Connector
Synthesized BFO	455 ±8 kHz in 10 Hz steps
Noise Figure	< 15 dB
Dynamic Range	RF: > 180 dB/Hz

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TABLE 1-1. RA6790/GM HF RECEIVER SPECIFICATIONS (Cont.)

Sensitivity (500 kHz to 30 MHz):	
1. SSB	−113 dBm (0.5 μV) for 10 dB (S+N)/N Ratio.
2. AM	−99 dBm (2.5 μV) for 10 dB (S+N)/N Ratio in a 6 kHz bandwidth.
Overall Selectivity (Standard Mechanical Filter Complement)	A wide variety of mechanical and crystal filters is available for optional requirements such as general purpose, low ripple, low shape factor, controlled delay, or linear phase. The standard filter complement is provided by six mechanical filters that are supplied with the receiver. This includes two sideband filters and four symmetrical filters. The seventh filter slot is linked in order to provide a fifth symmetrical bandwidth defined by the selectivity of the 20 kHz roofing filters. The -3 dB and -60 dB bandwidths are defined as follows: LSB/USB -3 dB >450 Hz to >3000 Hz; -60 dB >-600 Hz to <4300 Hz. The remaining five bandwidths are symmetrical: BW1 -3 dB >300 Hz, -60 dB <2 kHz; BW2 -3 dB >1 kHz, -60 dB <4.5 kHz; BW3 -3 dB >3.2 kHz, -60 dB <8 kHz; BW4 -3 dB >6 kHz, -60 dB <14 kHz; BW5 -3 dB >20 kHz, -60 dB <80 kHz
Intermodulation (Out of Band)*	For signals 100 kHz or more from receiver tuned frequency the third order intercept point is greater than +30 dBm. Second order intercept point is greater than +60 dBm. *Below 1.5 MHz these limits may be exceeded.
Intermodulation (In Band)	Better than −50 dB for two −10 dBm input signals within the IF passband when measured at the IF or line AF output.
Cross Modulation	The level of a 30% modulated signal, 50 kHz off-tune necessary to cross modulate an on-tune carrier to a depth of 3% shall be greater than +21 dBm (2.5 volts).
Blocking	1. On Tune: Less than 10% distortion for +13 dBm (1 volt) 30% Modulated AM input signals. 2. Off Tune: 1 dB on a 30% modulated on-tune signal when in the presence of a +23 dBm (3 volt) unmodulated carrier 50 kHz off-tune.
Reciprocal Mixing	The apparent noise appearing at the receiver input when in a 3 kHz bandwidth, caused by a 0 dBm signal 100 kHz off tune is less than −100 dBm.

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TABLE 1-1. RA6790/GM HF RECEIVER SPECIFICATIONS (Cont.)

Image and Spurious Rejection	Greater than 80 dB, for signals at least ±50 kHz from tuned frequency.
Internal Spurious Responses	< −124 dBm
Outputs	1. IF: Frequency 455 kHz, Impedance 50 Ohms. Level - 10 dBm nom. Connector BNC. 2. Following outputs available at rear panel audio connector (25 pin Type D). AF: 100 Hz to 16 kHz for −3 dB. a. 1W nominal into 8 Ohm load. Distortion < 3% at 500 mW. b. Monitor: Metered AF line output. 1 mW, 600 ohms balanced <2% distortion. All receiver modes selectable at front panel. c. Line 1. AF line output. 1 mW, 600 ohms balanced <2% distortion. Operable only with ISB option. All modes select at front panel except LSB. d. Line 2. AF line output. 1 mW, 600 ohms balanced <2% distortion. Operable only with ISB option, OSB mode. AGC: Diversity Connection with ground which provides dc voltage 10 volts to 4 volts to signal levels between threshold and +110 dB. Similar connection for ISB channel when fitted. Fault: Indication of fault condition is available at the rear panel. 3. Phone: 30 mW into 600 Ohm load. Distortion <3% at 10 mW. Connector: Front Panel Phone Jack 4. REFERENCE OUT: Selectable TCX0 Reference frequency of either 1, 5, or 10 MHz (selected by links on A8 assembly) Connector: Rear panel BNC
Environmental	1. Operating Temperature: 0°C to 50°C 2. Operating Humidity: 10% to 85% non-condensing. 3. Altitude: Operation to 15,000 ft. 4. Bench Handling: MIL-STD-810C, Method 516.2, Procedure V 5. Vibration: MIL-STD-810C. Method 514 2 Procedure X 6. Storage Conditions: a. Temperature Range: −40°C to +70°C b. Relative Humidity: 10% to 95% non-condensing. c. Altitude: Up to 40,000 feet d. Fungis: Fungi identified in MIL-STD-810, Method 508.1, Procedure I.
Power Consumption	Less than 40 Watts (nominal)
Power Requirements	115/230 Vac ±10%, 48 Hz to 420 Hz, single phase.
Dimensions	Suitable for 19 inch (48.3 cm) rack or desk top console mounting: Heights: 5.25 in. (13.33 cm) Width: 19 in. (48.3 cm) Depth: 18.5 in. (47 cm)
Weight (approximate)	32 lbs. (14.5 kg)

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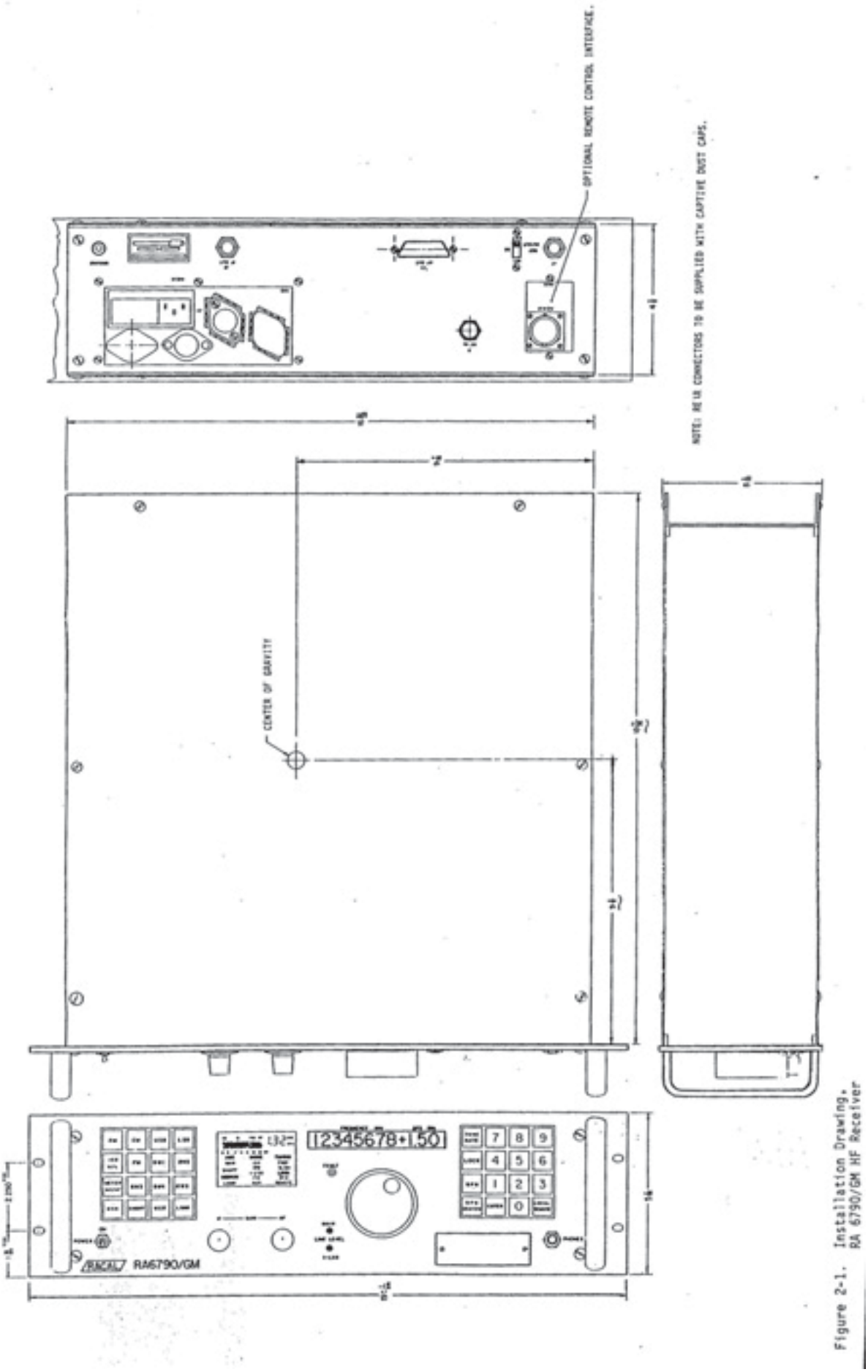

Figure 2-1. Installation Drawing, RA 6790/GM HF Receiver

SECTION II
INSTALLATION

2.1 UNPACKING AND INSPECTION

It is recommended that the shipping carton containing the RA7690/GM HF Receiver be examined for damage before the Receiver is unpacked. If damage to the carton is observable, try to have the carrier's agent present when the equipment is unpacked. If this is not possible, retain the shipping cartons and padding material for the carrier's inspection if damage to the equipment is evident after unpacking.

No special unloading equipment is required, except to handle the carton with normal care given to any shipping carton containing electronic equipment. Figures 2-1 and 2-2 show the critical dimensions and packaging details associated with the RA6790/GM HF Receiver. To unpack the Receiver, the following procedure should be observed.

1. Carefully open the top of the shipping carton and fold back the flaps.
2. Lift out the top foam cushion.
3. Carefully lift out the wrapped Receiver.
4. Remove the wrapping from the Receiver.
5. Carefully lift out the Receiver.
6. Place the Receiver on a convenient work bench.
7. Replace all packaging material back in the shipping carton. Save all material in the event that the Receiver must be reshipped.

See that the equipment is complete as listed on the packing slip. Contact your RACAL representative or RACAL Communications, Inc., Rockville, Maryland with details of any shortage.

The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is, therefore, ready for use upon receipt. After uncrating and checking contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections, and plug-in items which may have been loosened from their receptacles.

2.2 PREPARATION FOR RESHIPMENT AND STORAGE

If the RA6790/GM must be prepared for reshipment, the packaging methods should follow the pattern established in the original shipment. If retained, the original materials can be used to a large extent or will at a minimum provide guidance for the repackaging effort. The Receiver must be disconnected and removed from its mounting rack before being prepared for reshipment. The following procedures describe the recommended sequence.

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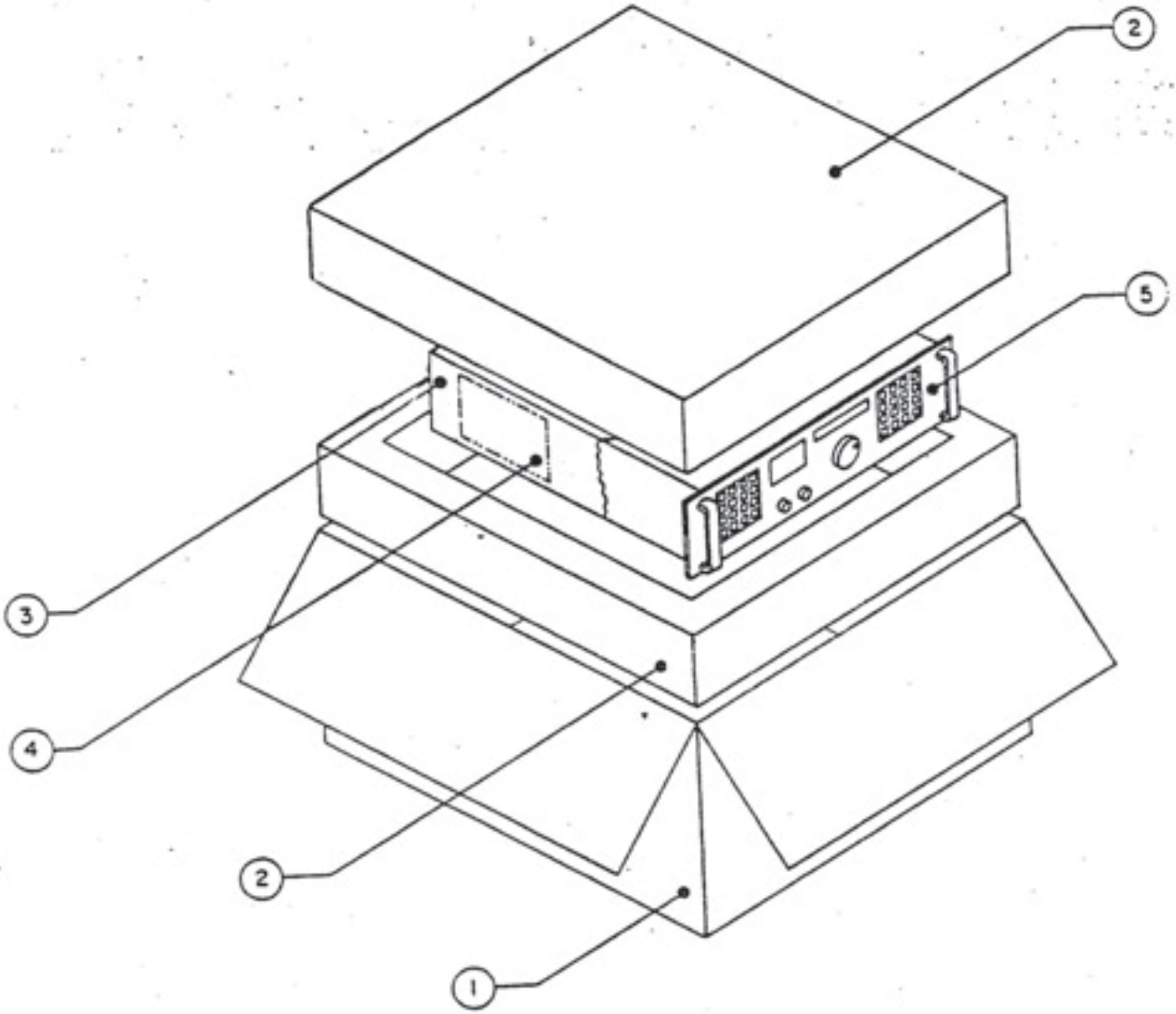

1. Exterior Container - 25-1/2" long by 23-1/2" wide by 10-1/2" deep.
2. Top and Bottom Cushions
3. Intimate Wrap.
4. Dessicant.
5. RA6790/GM Radio Receiver.

Figure 2-2. Packaging Details, RA6790/GM HF Receiver

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1. Disconnect primary power cable W18 from its primary power source. Disconnect the other end of the cable from A10J1 on the rear panel of the Receiver.

2. Disconnect the antenna cable from J1-RF IN on the rear panel.

3. Disconnect the ground strap from the GROUND lug located on the rear panel.

4. Remove any other equipment or cables connected to connectors or jacks on the rear panel.

5. Remove headphones, if they are inserted, from the PHONES jack located on the front panel.

6. Remove the four mounting screws from the front panel securing the Receiver to the mounting rack.

WARNING

The Receiver weighs approximately 30 pounds. Be careful as the unit is removed from the rack. Have a firm grip on the handles as the weight leaves the rack so that it does not drop, causing injury to legs or feet.

7. Grasp the Receiver by handles on the front panel and slide the unit out of the rack. Place the unit on a bench.

The unit may be housed (stored), from inclement weather, in any structure that will sustain a temperature between -40^{o} and $+70^{o}$C and a relative humidity of 10 to 95 percent. The unit has an indefinite shelf life stored under the above conditions except for the nickel cadmium battery contained on circuit module board A6A2.

2.3 INSTALLATION

The Receiver is designed to be mounted in a standard 19-inch rack. The sides of the Receiver have been drilled and tapped to accept standard slides. The use of slides, however, is optional and is dependent on the individual site requirements. If slides are installed, it is recommended that cable retractors be used to simplify extending the Receiver out of the rack. If the unit is rack mounted without the slides, access to the rear panel must be provided for connection of cables and test equipment. The power dissipation of the Receiver is approximately 50 Watts with most of the power as heat. In most installations, special cooling will not be required. The top and bottom covers on the Receiver, as well as the heat sinks on the rear panel, must be unobstructed to permit proper air circulation. Critical dimensions of the RA6790/GM Receiver are shown in Figure 2-1.

2.3.1 Rear Panel Jacks, Switches and Connectors

Access to the rear panel should be allowed so that input and output connections can be conveniently made or changed if desired. All connections except for the headphones are made from the rear of the Receiver. A brief description of each rear panel switch and connector indicating function and input/output parameters is presented. Figure 2-3 presents the rear panel view of the Receiver showing the locations of the jacks, switches and connectors.

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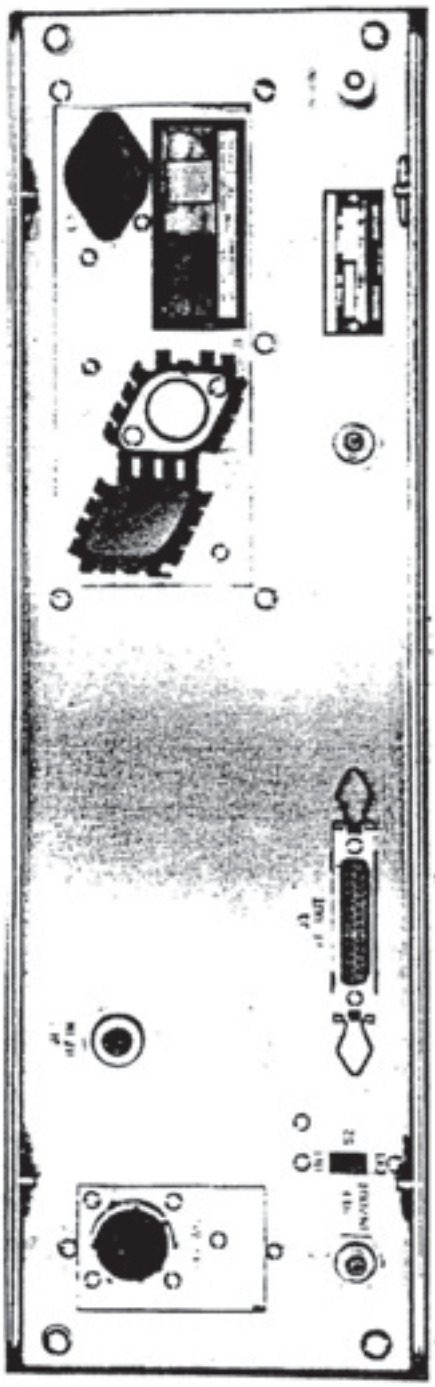

Figure 2-3. Rear Panel Jacks, Switches and Connectors

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2.3.1.1 A10J1 Power Input Connector and Voltage Selector/Fuse Block Assembly

This multi-function assembly contains a three prong male power receptacle for attaching the power input cable, W18; hinged plastic FUSE PULL lever; line voltage select PC wafer and line fuse, F1. The power input cable is type BELDEN 17250. **CAUTION:** Verify that the PC wafer in A10 J1 on receiver rear panel matches available line voltage.

2.3.1.2 RF IN J1 Connector

The RF input from the antenna to the Receiver is made through the rear panel connector, J1. This connector is a standard N-type female connector and will mate with any standard N-type male connector. The input impedance at the connector is 50 ohms, unbalanced, with a VSWR of 2:1 over the operating frequency range of the Receiver.

2.3.1.3 IF OUT J2 Connector

The second IF output signal at 455 kHz is supplied by this female BNC-type connector which will mate with any standard male BNC-type connector. The output signal level at the connector is −10 dBm ±5 dB for all CW input signals within the range of −107 dBm to +13 dBm with AGC selected. The impedance of the IF output is 50 ohms with a VSWR of 1.5:1.

2.3.1.4 AF OUT J3 Connector

This rear panel output connector is a 25-pin D-type connector providing audio, AGC and fault status outputs. The audio output frequency response at this connector is within 3 dB between frequencies of 100 Hz and 16 kHz. The following audio outputs are available:

1. Loudspeaker Output. An unbalanced output capable of < 3% distortion at 500 mW for 1W nominal into an 8 ohm load.

2. Monitor Line Output. A metered line output for receivers which do not contain the ISB option. Provides a 1 mW output at 600 ohms. The amplitude level is adjustable from the front panel.

3. Line 1. Line output for non-operating ISB mode when the ISB is installed. Output is 1 mW at 600 ohms balanced.

4. Line 2. Line output for the LSB component in the ISB operating mode. Output is 1 mW at 600 ohms balanced.

5. PHONES. This unbalanced output is capable of 10 mW at 600 ohms and is available through a front panel jack.

If the Receiver is not equipped for ISB operation, the Line 1 and Line 2 outputs are not used. The Monitor Line output. Loudspeaker output, and the front panel PHONES jack provide the audio output for the Receiver for all operating modes. When the Receiver is equipped for and is operating in the ISB mode, the Line 1 output will contain the USB audio and the Line 2 output will contain the LSB audio. The Monitor Line and Loudspeaker outputs, along with the front panel PHONES jack will provide either USB or LSB audio as controlled by the front panel ISB U/L pushbutton. With the Receiver equipped for ISB operation but not operating in the ISB mode, the

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Line 1, Monitor Line, and Loudspeaker outputs, along with the front panel PHONES jack, provide the audio.

Other outputs available at this connector are the AGC and Fault indicator outputs.

The Main IF and ISB-LSB AGC Monitor/Input terminals may be used to control the AGC for diversity combining or to monitor the AGC voltage. For diversity combining, the Main IF AGC signal (on pin 21 of J3) of one receiver may be connected to pin 21 of the second receiver. If the receiver is equipped for ISB operation, pin 22 of one receiver may be connected to pin 22 of the second receiver. The AGC circuits in both receivers will automatically respond to the proper signal. The Fault Indicator output will be high (logic 1, +2 Volts to +5 Volts) when a fault is not present in the Receiver. This output will go low (logic 0, 0 Volts to +0.8 Volts) when one of the synthesizer circuits has failed or if a parity error is detected during remote control (optional).

2.3.1.5 REF IN/OUT J7 Connector

This rear panel connector is used in conjunction with Slide Switch, S2. Depending on switch position, the Receiver will either accept an external 1 MHz reference input or supply a 1 MHz reference output through J7. The circuitry has an input impedance of 50 ohms and will operate with peak-to-peak signal levels of 1.0V, ±0.5V. The J7 connector will mate with any standard male BNC-type connector. Additionally, provision for changing the reference frequency to either 5 MHz or 10 MHz is available by making link changes (Refer to Paragraphs 2.3.4 and 2.3.4.5, Receiver System Connections) on the A8 assembly.

2.3.1.6 A6A1W1J1 Remote Control Interface Connector

This optional connector is a round, 26-pin MIL-Type MC3723-02R-1626N and permits the Receiver to be operated from a remote control device. A mating connector is supplied with the A6A1 Remote Option. Depending on which interface is required, pin connections, jumper options and baud rate selection must be appropriately set. (Refer to Paragraphs 2.3.4 and 2.3.4.6, Receiver System Connections.)

2.3.1.7 INT EXT S2 Slide Switch

Setting this switch to the INT position selects the internal time base for the Receiver and provides the internal 1 MHz reference output at connector J7. Setting the switch to the EXT position deactivates the internal reference so that an external signal may be applied to J7. The Receiver is normally shipped from the factory with the 1 MHz reference present, however, provision for changing to 5 MHz or 10 MHz is available by changing links on the A8 assembly. (Refer to Paragraph 2.3.4 and 2.3.4.5.)

2.3.1.8 GROUND Lug

A GROUND Lug is located at the lower right corner of the receiver rear panel. Ensure that adequate grounding techniques are employed when operating, installing options and performing maintenance functions on the RA6790/GM Receiver.

2.3.1.9 PHONES Jack

This output is intended to drive a 600 ohm headphone set and provides an audio output for the Receiver for all operating modes.

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2.3.2 Installation Options

The external options associated with the Receiver include plug-in or solder-in IF bandwidth filters, independent sideband (ISB) operation, and operating the Receiver through a remote control device. One or more of the plug-in or solder-in filters must be installed before the Receiver can operate. The ISB and remote control capabilities, however, are optional. Because of the different possible filter combinations and the options, it is recommended that a receiver configuration chart or log book be maintained for each Receiver. The configuration chart or log book would list the IF bandwidth filters currently installed in the Receiver, the operating options, the type of remote control interface, as examples.

In addition, an internal option of operating the RA6790/GM Receiver with a 1, 5 or 10 MHz reference is available by changing links on the A8 assembly.

2.3.3 RA6790/GM Receiver Options Installation Procedures

The installation procedures for the Receiver may be logically divided into three steps: (1) Installation of the primary operating options to include the plug-in (solder-in) filters, independent sideband and remote control interface; (2) making the required system connections; and (3) installation of the Receiver in an operational position. Paragraphs 2.3.3.1 through 2.3.4.6 detail the installation steps necessary for preparing the RA6790/GM HF Receiver for operation. Figures 2-4 through 2-9 are photographs of the details associated with installing the receiver operating options.

2.3.3.1 Optional IF Bandwidth Filters

The standard RA6790/GM Receiver is supplied with soldered-in mechanical filters and input and output shunt capacitors, (Table 6.1, Section VI). If conversion to plug-in filters is desired, actual removal of these items should be performed at the RACAL Communications, Inc. factory location in Rockville, Md.

The Receiver can be supplied with from 1 to 7 plug-in filters. Table 2-1 lists all the optional filters available. Mounted on the A4 board, the filters are accessible from the top of the Receiver. To gain access to the A4 board, loosen the six quarter-turn fasteners holding the top cover to the Receiver and carefully remove the top cover. A retaining cover is used with the crystal filters. Remove the three screws holding this cover to the chassis and remove the cover. Figure 2-4 illustrates the seven filter slots on the A4 board.

If a receiver configuration chart has been prepared for this particular Receiver, refer to the chart and determine if the Receiver is to be operated with the ISB option. If the receiver configuration chart was not prepared, determine if the ISB option is to be included by checking the shipping data or the station manual, as appropriate. When operating with the ISB option, both upper and lower sideband filters must be installed in the Receiver, and the lower sideband filter must be installed in the FL1 position. If the ISB option is not used, either a lower sideband filter or symmetrical sideband filter may be installed in the FL1 position. When a lower sideband filter is installed, the companion upper sideband filter must be installed in one of the remaining filter positions. If a symmetrical sideband filter is used, the Receiver will use the filter installed in the FL1 position for both sidebands by making the appropriate frequency offsets to the first and last local oscillators. The remaining filters may be installed in any sequence in filter positions FL2 through FL7. However, in order to simplify system operation and troubleshooting, it is recommended that a format be established and used for all Receivers at a particular site.

Once the filter complement and arrangement has been determined, the following procedure should be used to insert the plug-in filters into the Receiver. Refer to Figures 2-4 and 2-5.

1. Working from the front of the Receiver, position the filter to be used for LSB operation over filter position FL1 (the filter position closest to the rear of the Receiver). Make certain that the large pins are aligned with the large sockets and the smaller pins are aligned with the smaller sockets.

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TABLE 2-1. RA6790/GM OPTIONAL BANDPASS FILTER LIST

*Mechanical Filters. All Others are Crystal Filters.

Bandwidth	Description	Shape Factor 3 dB: 60 dB	Differential Delay μS	Racal Number
*0.3 kHz	Symmetrical BPF	1:6.7	–	07883-1
*1.0 kHz	Symmetrical BPF	1:4.5	–	07883-2
*3.2 kHz	Symmetrical BPF	1:2.7	–	07883-3
*4.0 kHz	Symmetrical BPF	1:2.5	–	3600001
*5.0 kHz	Symmetrical BPF	1:2.5	–	3600002
*6.0 kHz	Symmetrical BPF	1:2.3	–	07883-4
*450 Hz to 3000 Hz	ISB/USB BPF	1:1.92	–	07883-5
*450 Hz to 3000 Hz	ISB/LSB BPF	1:1.92	–	07883-6
*350 Hz to 2700 Hz	USB BPF	1:1.66	–	08669
*300 Hz to 2200 Hz	USB BPF	1:1.97	–	08771
1.0 kHz	Symmetrical BPF	1:6	25	3600003
3.0 kHz	Symmetrical BPF	1:6	13	3600004
6.0 kHz	Symmetrical BPF	1:6	10	3600005
1.0 kHz	Symmetrical BPF	1:2.5	1080	3600006
3.0 kHz	Symmetrical BPF	1:2.5	360	3600007
6.0 kHz	Symmetrical BPF	1:2.5	180	3600008
0.125 kHz	Symmetrical BPF	1:5.33	–	08699
0.4 kHz	Symmetrical BPF	1:6.2	–	08406
1.2 kHz	Symmetrical BPF	1:6	–	08407
6.8 kHz	Symmetrical BPF	1:3.3	–	08408
350 Hz to 3050 Hz	ISB/LSB BPF	1:1.6	800	08409
350 Hz to 3050 Hz	ISB/USB BPF	1:1.6	800	08410
0.4 kHz	Symmetrical BPF	1:2.5	2000	08411
1.2 kHz	Symmetrical BPF	1:2	1000	08412
3.24 kHz	Symmetrical BPF	1:1.33	1000	08413
6.8 kHz	Symmetrical BPF	1:2	1000	08414
16.0 kHz	Symmetrical BPF	1:2	40	08415
0.5 kHz	Symmetrical BPF	1:6	80	08416
1.0 kHz	Symmetrical BPF	1:6	40	08417
2.0 kHz	Symmetrical BPF	1:6	20	08418
3.0 kHz	Symmetrical BPF	1:6	20	08419
6.0 kHz	Symmetrical BPF	1:6	20	08420
0.075 kHz	Symmetrical BPF	1:6.67	–	08589

2. Carefully push down on the filter to insert the pins into the sockets. Relatively light pressure is required to insert the pins into the sockets. If the filter does not easily slide into place, recheck the pin/socket alignments.

3. Insert the appropriate filters into filter positions FL2 through FL7 (as required), using the procedures described in steps 1 and 2.

4. After all filters have been inserted, visually inspect the filters to insure that they are properly seated. The bottom of the filters should be flat against the surface of the A4 board.

5. Replace the RF shield over the filters and secure the shield in place by tightening the three screws.

NOTE

If the Receiver is to be equipped for operation from a remote control device or in the ISB mode, continue with the procedures described in Paragraphs

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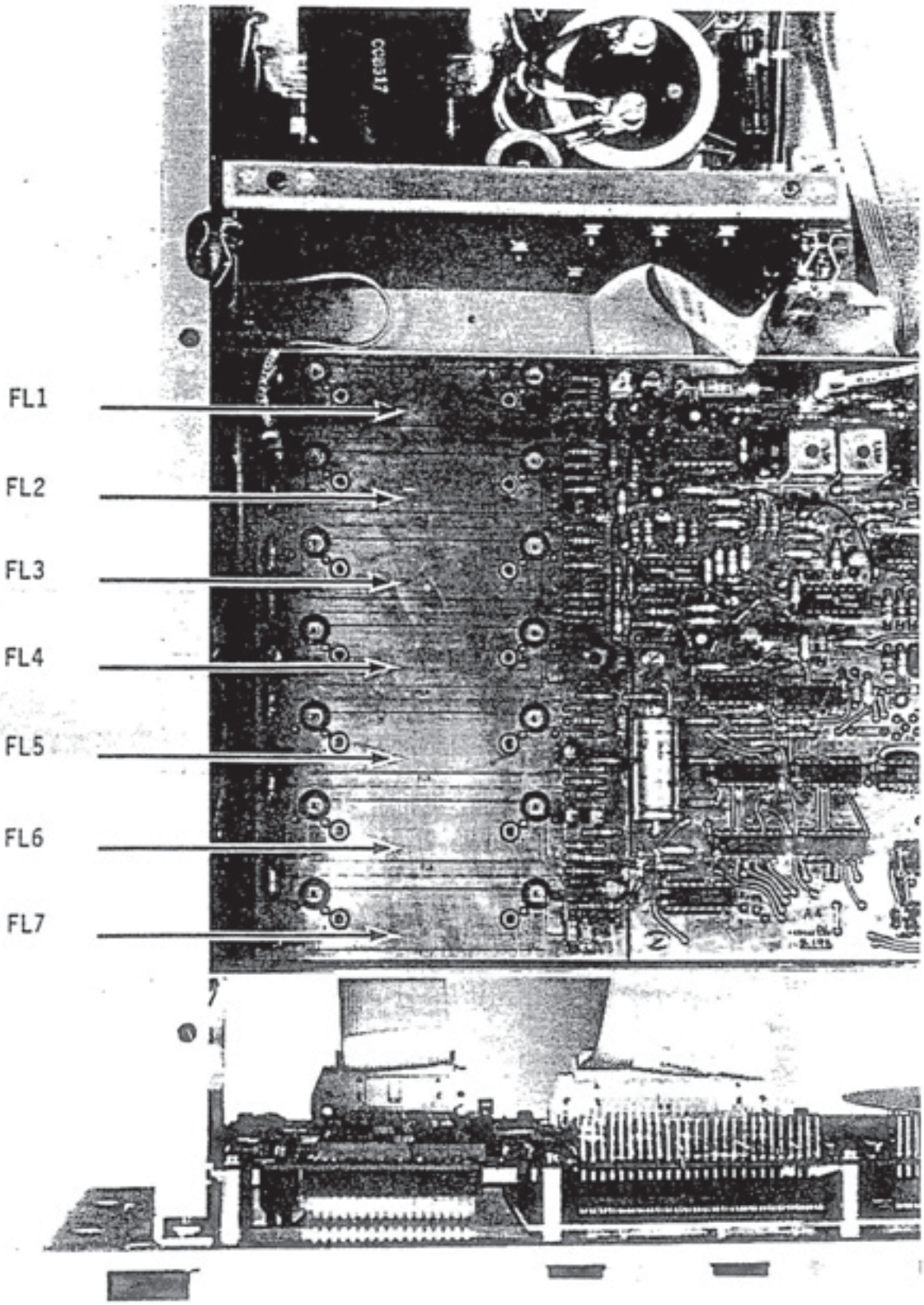

Figure 2-4 Location of IF Bandwidth Filter Slots

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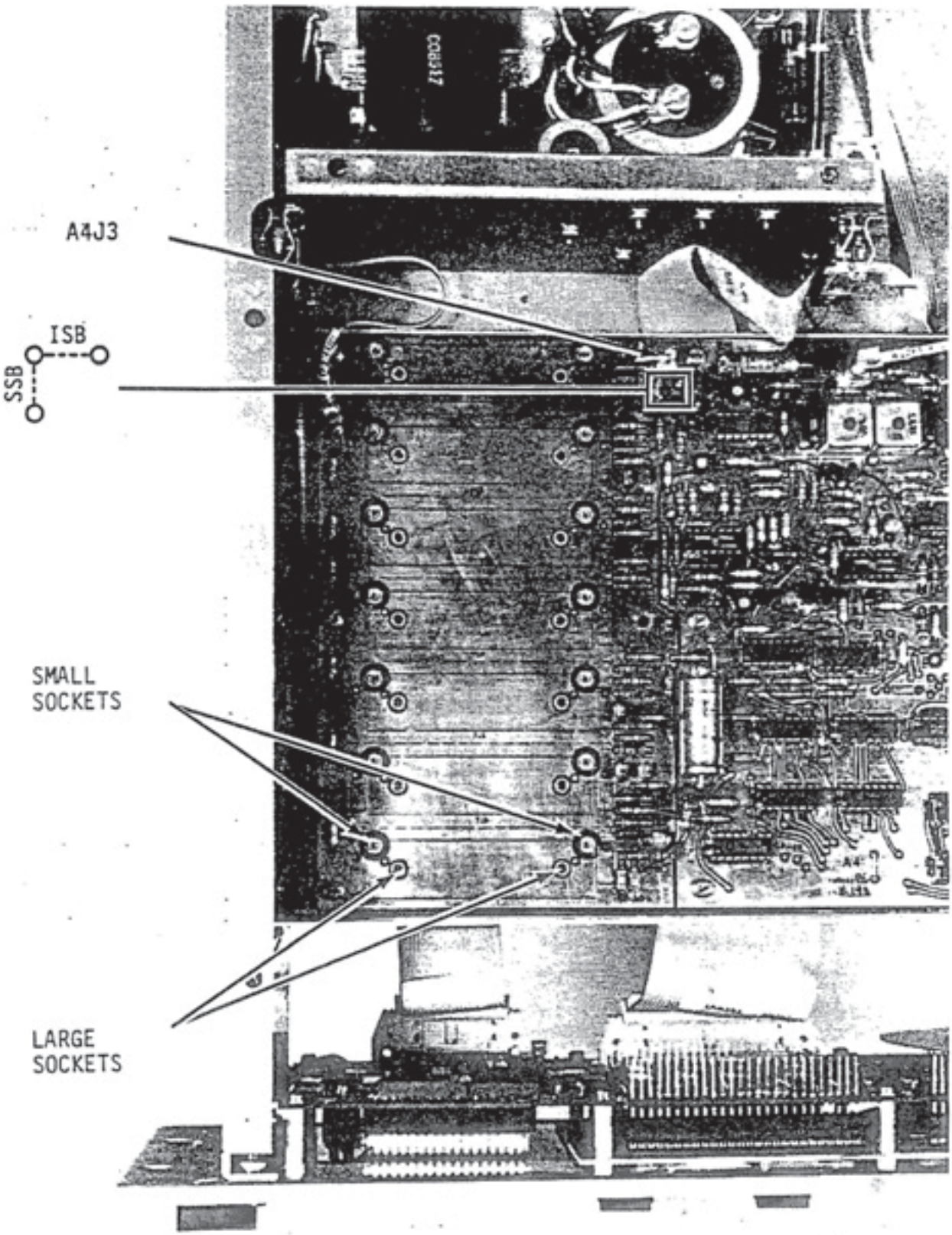

Figure 2-5. Location of Filters and Jumpers, A4 Circuit Card Assemby

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2.3.3.2 and 2.3.3.3. If the Receiver is not to be equipped with these two options, replace the top cover on the receiver chassis, and proceed to Paragraph 2.3.3.4, Line Level Adjustments.

2.3.3.2 Remote Control Serial Asynchronous Interface

When the Receiver is operated with the remote control option, the A6A1 circuit card assembly must be installed in the Receiver. In order to install this card, the A6A2 circuit card assembly must be removed from the Receiver and mated with the A6A1 card. The two cards are then inserted back into the Receiver as an assembly. The following procedure details the steps necessary to install the cards.

1. Working from the front of the Receiver, disconnect the A9W1 cable assembly from the A6A2 card. This cable assembly connects to A6A2J1 located on the front of the A6A2 card. Figure 2-6 illustrates the A6A2 and A6A1 circuit card assemblies installed in the Receiver and the location of A9W1.

2. Remove the three screws located along the top edge of the A6A2 card and carefully remove the card from the Receiver.

CAUTION

Do not place the A6 circuit card assembly on any conductive material. Failure to comply may result in shorting the battery contained on this card.

3. Check the rear panel of the Receiver. A blank plate may be covering up the hole (located on left hand side of the rear panel) for the remote control interface socket. If the blank plate is present, remove the two screws holding the plate and remove the plate.

4. A hard-wired link, LK1, must be removed from the A6A2 card when the remote control option is used. The link is physically located between U1 and U2 (the two 40-pin LSI chips located near the J2 connector). Use a pair of cutters (or a low wattage soldering iron) to remove the link. Refer to Figure 2-7 for the location of the link.

5. There are a total of 6 different mechanical links located on the A6A1 circuit card assembly that must be installed according to the interface to be used. Table 2-2 lists the mechanical links required for each interface. Use a low wattage soldering iron to install or remove the links as required. Refer to Figure 2-8 for the location of the links.

TABLE 2-2. LINK DESIGNATIONS, REMOTE CONTROL INTERFACE

Link Designation	188C/232C/423 Interface	RS422 Interface
LK1	Install	Install
LK2	Remove	Remove
LK3	Install	Remove
LK4	Install	Remove
LK5	Install	Remove
LK6	Remove	Install

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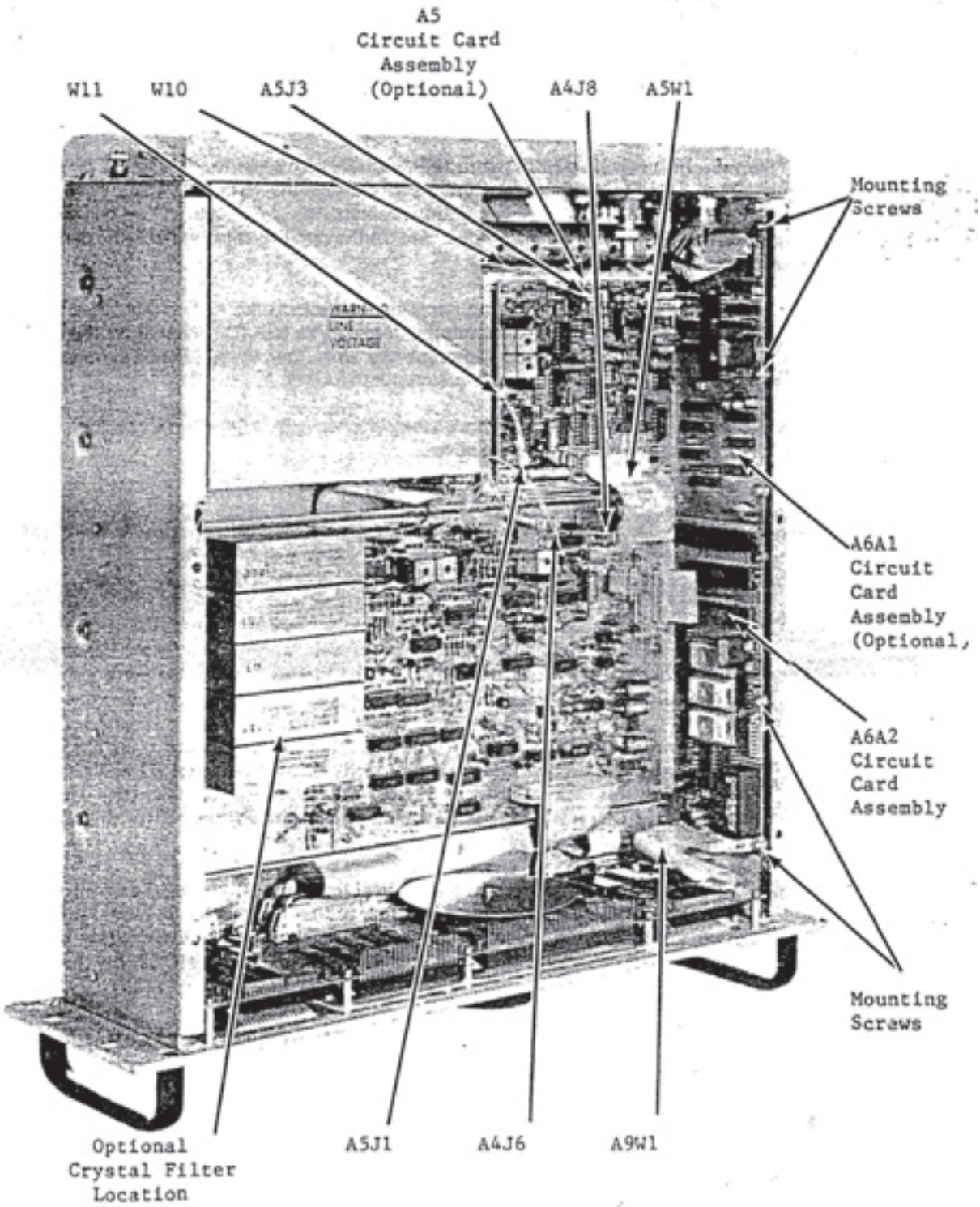

Figure 2-6. Receiver Options, Installation Detail

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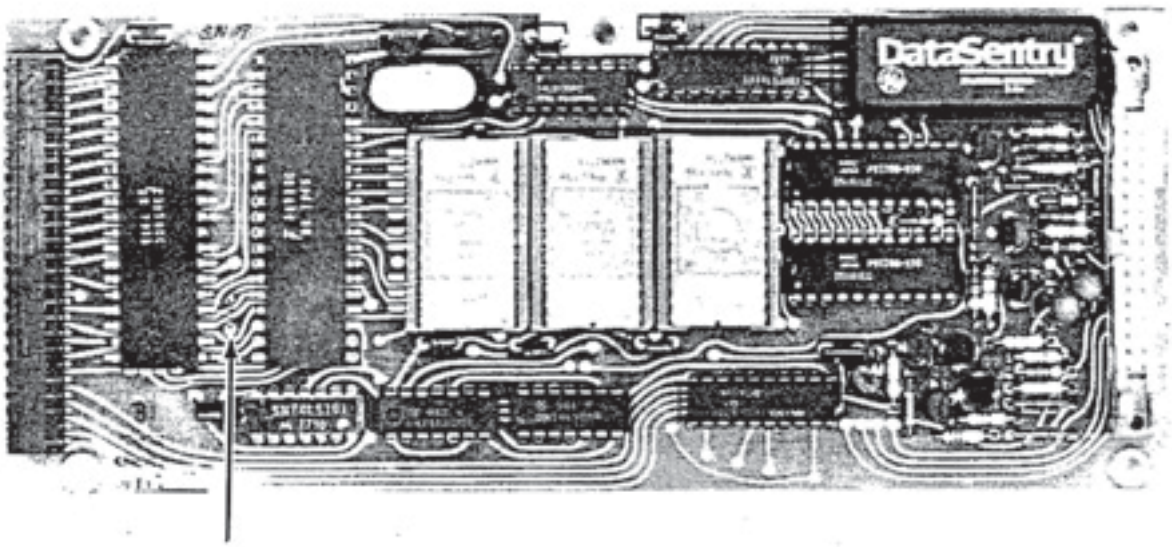

Figure 2-7. A6A2 Circuit Card Assembly Jumpers

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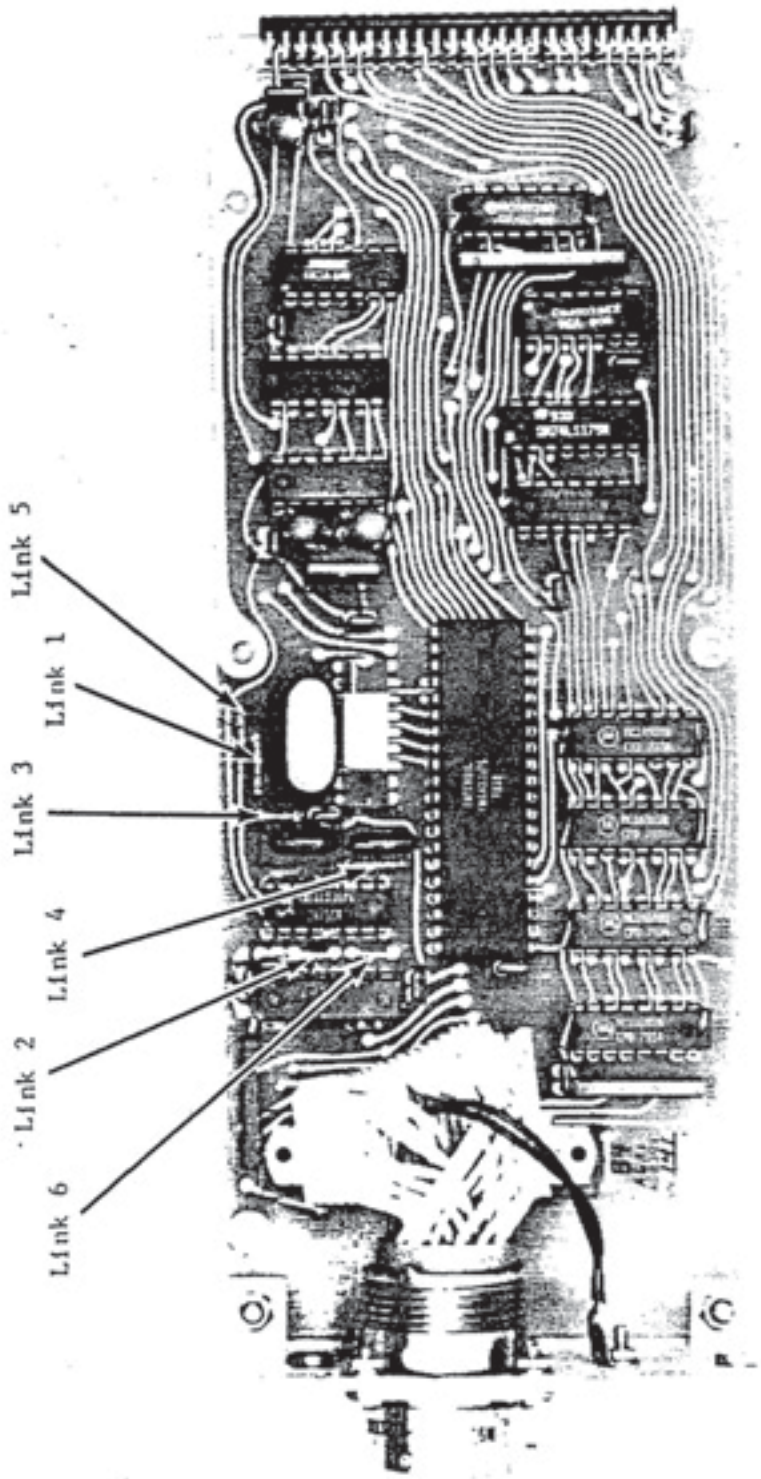

Figure 2-8. A6A1 Circuit Card Assembly Jumpers

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6. Align the 50-pin male connector on the A6A1 circuit card assembly with the 50-pin female connector on the A6A2 circuit card assembly as shown in Figure 2-9. Mate the two connectors.

7. Carefully place the two cards into the receiver chassis. Make certain the remote control interface connector (A6A1W1J1) clears the hole in the rear panel.

8. Position the two cards on the card guide attached to the receiver chassis. Secure the cards with 6 screws (3 screws on each card) to the side of the chassis. Secure the interface connector to the rear panel with two screws. Figure 2-6 illustrates the two cards installed in the Receivers.

9. Reconnect the A9W1 cable assembly (removed in step 1) to connector A6A2J1.

NOTE

If the Receiver is to be equipped for operation in the ISB mode, continue with the procedure described in Paragraph 2.3.3.3. If the ISB option is not to be installed, replace the top cover on the receiver chassis and proceed to Paragraph 2.3.3.4, Line Level Adjustments.

2.3.3.3 Independent Sideband (ISB)

If the Receiver is to be operated in the ISB mode, the A5 circuit card assembly must be installed in the Receiver. The A5 card is located towards the rear of the Receiver, between the A1 assembly and the A4 circuit card assembly as shown in Figure 2-6. The following procedure details the steps necessary to install the A5 circuit card assembly. Refer to Figures 2-5 and 2-6 for the location of cables and connectors.

1. Place the metal baseplate shield (curved edge upwards) on the four standoffs and secure with four screws through the standoffs.

2. Position the A5 circuit card assembly so that the ribbon cable is near the J8 connector on the A4 circuit card assembly. Secure the A5 circuit card assembly to the metal baseplate with 4 screws.

3. Plug in the ribbon cable (A5W1) from the A5 card into J8 on the A4 board. Connect coaxial cable W10 between A4J6 and A5J3. Connect coaxial cable W11 between A4J3 and A5J1.

4. The mechanical jumper on the A4 circuit card assembly must be properly positioned for ISB/SSB operation. The jumper, designated LK1, is physically located to the right of filter position FL1 when looking from the front of the Receiver. (Refer to Figure 2-5.) With the A5 circuit assembly installed, the jumper must be connected across the two terminals designated ISB.

NOTE

Upon completing all required installation options procedures, it is recommended that the Line Level Adjustment procedure be performed as outlined in Paragraph 2.3.3.4. Upon completing this adjustment procedure, the RA6790/GM Receiver Options Installation Check as described in Section III, Paragraph 3.3.1 should be performed. After completing this operational check, it is suggested that the System Connection be made in accordance with the procedure listed in Paragraphs 2.3.4 through 2.3.4.6.

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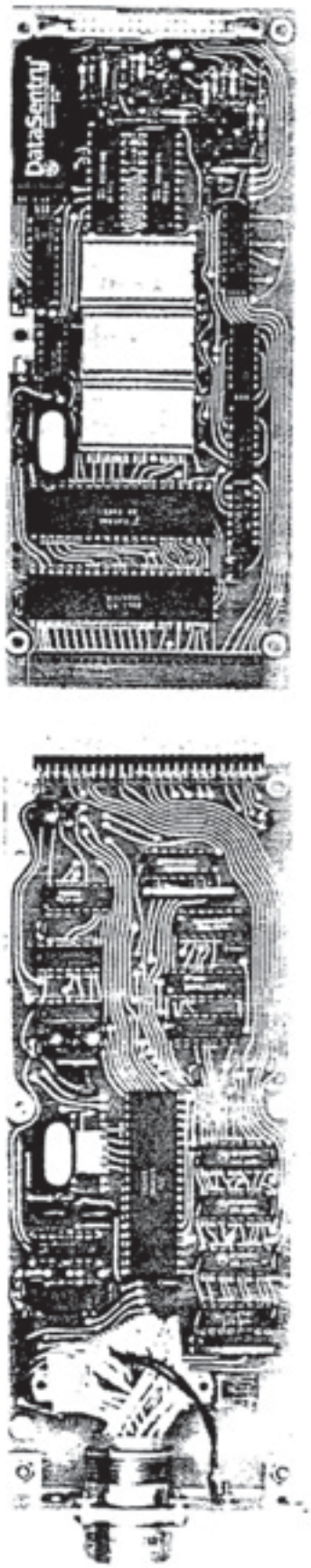

Figure 2-9. Mating A6A1 and A6A2 Circuit Card Assemblies

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2.3.3.4 Line Level Adjustments

The following procedures are detailed for adjustment of the audio line level, required upon installation of the Receiver.

1. For MAIN LINE LEVEL Adjustments:

   a. Set the following controls as indicated:

POWER switch	ON
AGC	SHORT
METER switch	AF
MODE	AM (depress AM pushbutton switch on lefthand keypad until the word AM is displayed under the word MODE in the Mode LCD).
BW	Approximately 6 kHz

   b. Connect the AM output (with modulation set for 30%) from an RF signal generator (HP8640, or equivalent) set to a frequency of 3.50000 MHz and an output of −97 dBm, to the RF IN connector J1 on the rear panel.

   c. Set the receiver frequency to 3.50000 MHz.

   d. Using a screwdriver, adjust the MAIN LINE LEVEL potentiometer on the receiver front panel for 1 mW audio output level, as indicated by the 0 dB line on the AF meter scale in the Mode LCD.

   e. Turn POWER switch to off and disconnect the generator.

2. For I-LSB LINE LEVEL Adjustment:

   a. Set the following controls as indicated:

POWER switch	ON
AGC	SHORT
METER switch	AF
MODE	I-LSB (depress ISB U/L switch on lefthand keypad once or twice until the I-LSB word is displayed under the word MODE in the Mode LCD).
BW	Approximately 6 khz

   b. Connect the AM output (with modulation set for 30%) from an RF signal generator (HP8640, or equivalent) set to a frequency of 3.50000 MHz and an output of −97 dBm, to the RF IN connector J1 on the rear panel.

   c. Set the receiver frequency to 3.50000 MHz.

   d. Using a screwdriver, adjust the I-LSB LINE LEVEL potentiometer on the receiver front panel for a 1 mW audio output level, as indicated by the 0 dB line on the AF meter scale in the Mode LCD.

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NOTE

The USB line level was adjusted when the MAIN LINE LEVEL was set since the USB AF uses the main AF channel when the Receiver is in the USB mode.

e. Turn POWER switch to off and disconnect the generator.

2.3.4 RA6790/GM Receiver System Connections

System connections for the Receiver are based on the individual site requirements and the options associated with a Receiver. The site requirements will determine the most effective method of installation. In some installations, it may be easier to pre-wire an entire equipment rack and then install the Receiver. In others, it may be easier to install the Receiver and then add the wiring. The following paragraphs detail the procedures associated with installing the Receiver. Figure 2-10 illustrates the connectors located on the rear panel of the Receiver.

2.3.4.1 Power Input Connections

A three-conductor power cord is supplied with the Receiver for connection to the power input plug. The connector has the following pin assignments, as viewed from the rear panel:

Left Pin:	LINE
Center Pin:	GROUND
Right Pin:	NEUTRAL

With the power cable unplugged from the Receiver, the clear plastic window can be slid over the three male power receptacle prongs. This exposes the line fuse and a hinged, plastic FUSE PULL lever. If the voltage shown does not match the available line voltage, remove the pc wafer and reinstall it so that the line voltage closest to the available line voltage is visible with the pc wafer in position. Install the fuse suitable for the line voltage: 1 amp slow-blow for 100V ac and 120V ac, or ½ amp for 220V ac and 240V ac. (An extra fuse may be installed in the alternate fuse holder, XF2 which is located internally on the A10 Power Supply Assembly.) Slide the clear plastic window back over the fuse and pc wafer portion of the fuse holder assembly and insert the power cable, W18, in the receptacle. Additionally, the Receiver should be grounded by attaching a suitable ground wire to the rear panel GROUND lug before the power cable, W18, is attached.

The Receiver is normally shipped from the factory configured for operation with a 120 volt, ± 10%, 48 to 420 Hz ac source. For receiver operation with a 240 volt source, the Receiver must be re-configured as follows:

1. Disconnect the Receiver from all system equipment and remove the power cord.

2. On the power input connector assembly A10J1: Slide the transparent protective cover to the left to expose the fuse; remove the fuse; remove the printed circuit wafer, and then replace the wafer with the required nominal operating voltage visible; replace the fuse and restore the protective cover to its original position and connect or re-connect the receiver system connections.

3. The unit is now ready for operation from the selected line voltage, ±10%.

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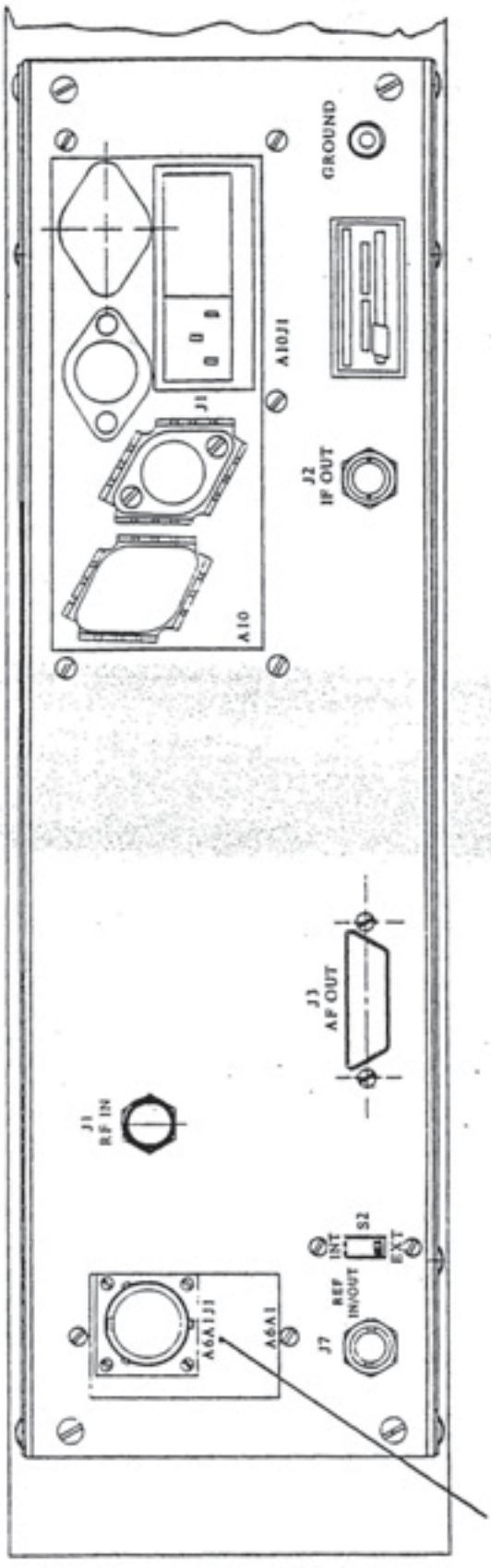

Figure 2-10. RA6790/GM Rear Panel System Connections

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CAUTION

The supply voltage should remain within 10% of the selected terminal voltage. A lower voltage can cause the internal regulation circuits to trip and a higher voltage can cause excessive internal temperatures.

2.3.4.2 RF INput Connector (J1)

The Receiver is shipped with a plastic dust cover over connector J1 which must be removed before the antenna connection can be made. Ensure that a suitable antenna is selected. The input impedance at the connector is 50 ohms, unbalanced with a VSWR of 2.1.

2.3.4.3 IF OUTput Connector (J2)

The IF Output Connector J2 located on the rear panel is shipped with a plastic dust cover which must be removed before connection. During operation, a 455 kHz frequency is supplied at this connector for connection to external equipment. Nominal level is –10 dBm into 50 Ohms.

2.3.4.4 AF OUTput Connector (J3)

A mating connector (Cannon type DB-25P) with a connector shell is supplied with the Receiver. Use the following procedure, and pin number/signal designation information in Table 2-3 to wire the connector.

1. Slide the connector shell over the cable to be used.
2. Solder the cable wires to the connector as required (refer to Table 2-3). The connector pin numbers are indicated on the front of the connector.
3. Slide the connector back into the connector shell. Place one of the spring clips on top of the connector with the curved edge pointing upwards. Secure the spring clip and the connector to the connector shell with the self-tapping screw. Repeat this procedure for the other side of the connector.
4. Connect the wired cable to the rear panel connector J3 and secure with two connector springs.

2.3.4.5 Reference Input/Output Connector (J7)

This BNC-type connector is used in conjunction with the INT/EXT S2 slide switch to accept an external reference source or provide an output of the internally generated reference signal. The reference frequency may be generated by a temperature controlled crystal oscillator (TCXO) located on circuit card A8, or by a frequency source external to the receiver. The receiver is normally shipped from the factory with a preset 1 MHz reference. Provision is made, however, for compatibility with a 5 or 10 MHz source through internal linkage on the A8, 2nd LO/BFO Synthesizer Board.

After determining the frequency source compatibility requirements, refer to Table 2-4 and make the following link changes on the A8 circuit board if required.

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TABLE 2-3. AF OUT J3 PIN CONNECTIONS

Pin Number	Signal Designation	
1 2 14	Output Center Tap Output	Line 1 Output (Used only with ISB Option). Provides USB output during ISB operation; AM/FM/CW/SSB output during non-ISB operation.
3 16 15	Output Center Tap Output	Line 2 Output (Used only with ISB Option). Provides LSB output during ISB operation.
4 5 17	Output Center Tap Output	Monitor Line Output. Provides AM/FM/CW/SSB output during non-ISB operation; provides switch controlled selection of USB or LSB during ISB operation.
18 6	Output Signal Ground	Loudspeaker Output. Same as Monitor Line Output.
7, 8, 9	Ground	
10,11,12,13 19,20,24,25	Not Connected	
21	Main IF Diversity AGC Monitor/Input	
22	ISB Lower Sideband Diversity AGC Monitor/Input	
23	Fault Indicator (Low indicates Fault)	

1. For 1 MHz operation, LK1 and LK2 are linked (E1 to E2, and E3 to E4 respectively).
2. For 5 MHz operation, LK2 ONLY is linked (E3 to E4).
3. For 10 MHz operation, LK1 ONLY is linked (E1 to E2).

TABLE 2-4. EXTERNAL/INTERNAL LINK OPTIONS

FREQUENCY SOURCE SELECTION	
1 MHz	Connect LK1 and LK2
5 MHz	Connect LK2
10 MHz	Connect LK1

Upon completing the required link changes, ensure that switch, S2 INT/EXT located on the rear panel is set in the appropriate position.

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2.3.4.6 Remote Control Serial Asynchronous Interface Connections (A6A1W1J1)

The Receiver is supplied with a mating connector for the remote control interface connector. Figure 2-11 illustrates the pin designations and assigned functions. The pins designated A through J vary in function according to the interface being used, as is shown in Table 2-5. The remaining pins K through c are the same for all the listed interfaces. Table 2-6 lists the baud rate selection bit associated with pins W through Z for different data rates (baud) selection. Table 2-7 lists the required link configurations on the A6A1 circuit card assembly for the different interfaces.

To make the required connections:

1. Slide the mating connector shell over the cable to be used for the remote control.

2. Solder the wires to the appropriate connector pins in accordance with Figure 2-11 and Tables 2-5 and 2-6 for the interface to be used. The connector pins are designated on the front of the connector.

3. After carefully checking all wiring, slide the connector into the connector shell and secure the cable clamp. Attach and secure the connector to A6A1W1J1.

4. Visually inspect the A6A1 circuit card assembly to insure that all jumpers are installed in accordance with Table 2-7.

NOTE

The MIL-STD-188C and RS-232-C interfaces are electrically compatible. The distinction between the two is the polarity definition for "MARK" or "LOGIC 1." RS-232-C defines "MARK" as a negative potential while MIL-STD-188C defines "MARK" as positive. Therefore, pin functions (Figure 2-11, Table 2-5) marked DATA IN A/DATA OUT A are "MARK" negative and DATA IN B/DATA OUT B are "MARK" positive.

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TABLE 2-5. DATA CONNECTION INTERFACE COMPATIBILITY

J1 Pins	MS188C	RS232C - RS423	RS422
A	System Gnd.	System Gnd.	System Gnd.
B	Not Used	Data Out A	Data Out A
C	Data Out Gnd.	Data Out Gnd.	Not Used
D	Data Out	Not Used	Data Out B
E	Jumper to 'F'	Not Used	Not Used
F	Jumper to 'E'	Data In A'	Data In A'
G	Data In Gnd.	Data In Gnd.	Not Used
H	Data In	Jumper to 'J'	Data In B'
J	Not Used	Jumper To 'H'	Not Used

TABLE 2-6. INTERFACE CONNECTOR BAUD RATE SELECTION

Data Rate Selection Bit				Data Rate
W	X	Y	Z	(Baud)
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1,200
1	0	0	0	1,800
1	0	0	1	2,000
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200

TABLE 2-7. A6A1 LINK CONFIGURATIONS

Link No.	188C/232C/423	422
LK1	Install	Install
LK2	Remove	Remove
LK3	Install	Remove
LK4	Install	Remove
LK5	Install	Remove
LK6	Remove	Install

TABLE 2-8. PARITY SELECT

No Parity	High	Open
Parity	Low	Ground
Even	High	Open
Odd	Low	Ground

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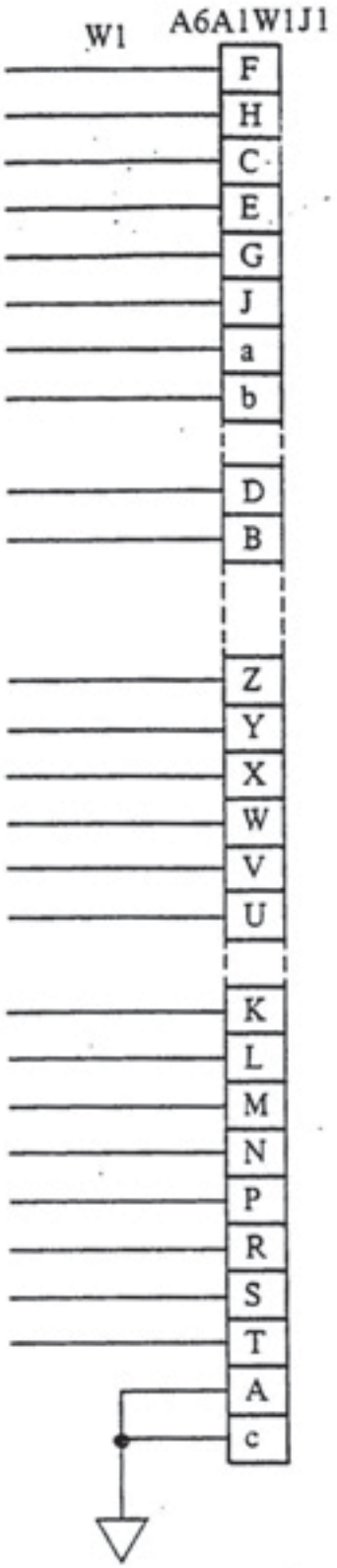

J1 Pins	Function
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A'
G	DATA IN GND
H	DATA IN B'
J	GND
K	RECEIVER NUMBER D1-1
L	RECEIVER NUMBER D1-2
M	RECEIVER NUMBER D1-4
N	RECEIVER NUMBER D1-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

Figure 2-11. Remote Control Connector Pin Designations and Functions

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Figure 3-1. Front Panel Controls and Indicators, RA 6790/GM

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SECTION III
OPERATION

3.1 GENERAL INFORMATION

All front panel controls, displays and indicators (Figures 3-1 and 3-2) are described in Paragraphs 3.2 through 3.2.11. Detailed operating procedures are presented in Paragraphs 3.3 through 3.3.3.2.

The front-panel keypad pushbutton switches are of the push-on type. When a pushbutton is depressed in a functional grouping, the Receiver will remain in that mode until a different selection is made. The front panel displays are of the liquid crystal type (LCD) indicating mode and frequency data.

The detailed operating procedures are presented in a logical sequence. Upon completing satisfactory installation of all required receiver options as described in Section II, Installation, Paragraphs 2.3.3 through 2.3.3.4, a Receiver Options Installation Check (Section III, Paragraph 3.3.1) should be performed. After performing this operating check and upon completion of any required system interface connections (Section II, Paragraph 2.3.4 through 2.3.4.6), a Receiver/System Interface Check (Section III, Paragraph 3.3.2) should be performed which will provide verification of all system connections. Local and Remote operating procedures are then detailed.

3.2 FRONT PANEL CONTROLS, DISPLAYS/INDICATORS

3.2.1 POWER-ON Toggle Switch

Double pole, single-throw toggle switch which provides on-off control for the Receiver by controlling primary power source to the power supply. During initial installation, be sure the line-voltage-select pc wafer on the rear panel matches the available line voltage before energizing the Receiver. Refer to Section II, Paragraph 2.3.4.1 for the voltage selection procedure.

3.2.2 Manual Tuning Knob

Optically coupled to a tuning encoder, the tuning knob provides selection of receiver operating frequency or BFO frequency. (Refer to TUNE RATE and BFO/BFO CENTER pushbutton controls.) The rate of change of the frequency depends on the speed the tuning knob is rotated and the rate of tune selected through the TUNE RATE switch. Clockwise rotation increases frequency, counterclockwise rotation decreases the frequency. Continuing to tune past the end of the range causes the Receiver to step to the opposite end of the band and to continue tuning in the same increasing or decreasing frequency direction.

3.2.3 IF GAIN Potentiometer

This front-panel control is used to establish the receiver gain control when the Receiver is operated in the manual mode, and to set the threshold level when the Receiver is operated in the automatic mode with a manually set threshold. Clockwise rotation increases IF signal level, while counterclockwise rotation decreases IF signal level. This control affects the IF signal level output through IF OUT connector J2.

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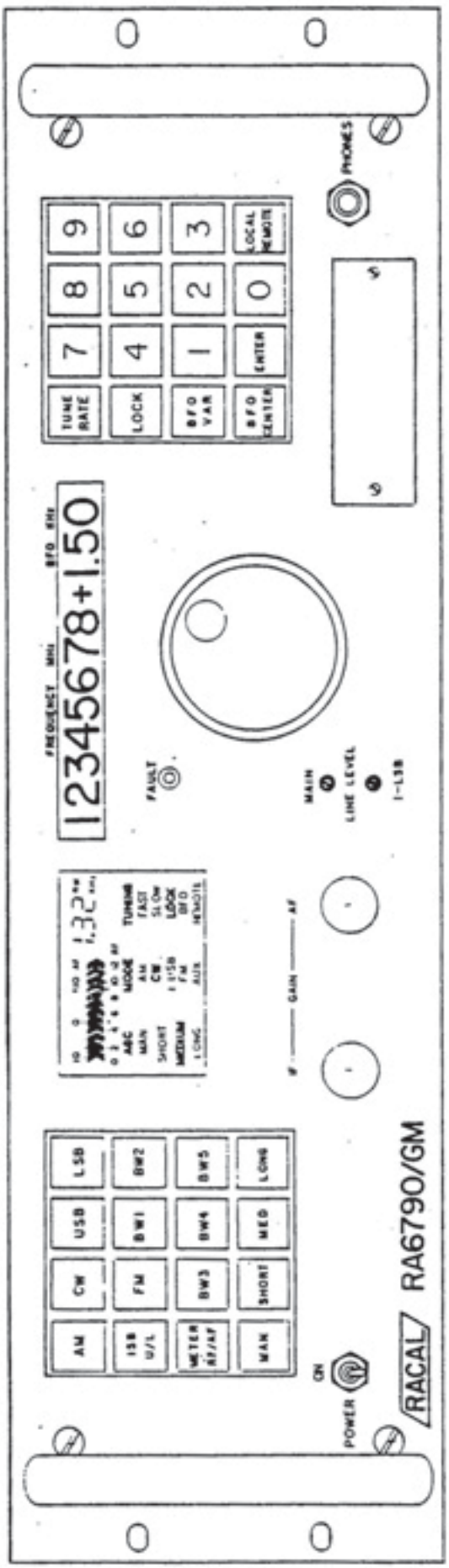

Figure 3-2. Front Panel Displays Detail

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3.2.4 AF GAIN Potentiometer

This front panel control is used to control the level of the receiver audio outputs. Clockwise rotation of the potentiometer increases loudness of the audio signal to the PHONES jack, while counterclockwise rotation decreases loudness. This control has no effect on audio signal level output through AF OUT connector J3.

3.2.5 MAIN LINE LEVEL Screwdriver-Set Potentiometer

This potentiometer is used to adjust the line level when the Receiver is operated in the AM, FM, CW, or SSB modes. If the Receiver is equipped to operate in the ISB mode (optional A5 circuit card assembly is installed), this control will adjust the line level of the upper sideband.

3.2.6 I-LSB LINE LEVEL Screwdriver-Set Potentiometer

This potentiometer is used to adjust the line level of the lower sideband when the Receiver is operated in the ISB mode (optional A5 assembly installed).

3.2.7 Lefthand Keypad Pushbutton Switches

a. Detection Mode: AM, CW, USB, LSB, ISB U/L, FM.

These pushbuttons are used to select the operating mode of the Receiver. (Refer to Section I, Figure 1-2.) The ISB U/L will be enabled only if the Receiver is equipped with the ISB option. If the Receiver is equipped with this option, depressing the pushbutton will activate both the USB and LSB channels simultaneously. If the front-panel display indicates I-USB, the PHONES jack will be connected to the upper sideband channel. Depressing ISB U/L a second time will change the display and connect the PHONES jack to the LSB channel. The monitor line and loudspeaker outputs, through rear panel connector J3, will also be switched with the ISB U/L pushbutton switch.

b. Bandwidth Pushbutton Switches: BW1, BW2, BW3, BW4, BW5

These pushbutton switches are used to select specific bandwidths within the Receiver. The Receiver is capable of accepting up to 7 plug-in IF bandwidth filters, and is usually configured with separate upper and lower sideband filters, leaving a capacity of up to five symmetrical filters. The upper/lower sideband filters will be automatically selected when the USB or the LSB mode is selected. The remaining filters (up to a total of 5) are selected by depressing the appropriate bandwidth selection pushbutton switches. BW1 will select the narrowest bandwidth, BW2 will select the next-wider bandwidth, and so on. Like the detection mode pushbutton switches, these are the push-on type, so that a new bandwidth is selected by depressing a different pushbutton switch.

c. METER RF/AF Pushbutton Switch

This pushbutton switch is used to change the front panel meter display to either an RF scale or an AF scale. The Receiver will always display either scale. Depressing the pushbutton will cause the display to switch either from RF to AF or AF to RF.

d. Gain Mode Pushbutton Switches: MAN, SHORT, MED, LONG

The Receiver is designed to operate with three different gain control modes: Manual, Automatic, and Automatic with a selectable threshold. Depressing the MAN pushbutton

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switch causes the MAN indication to appear in the display. If an automatic indication (SHORT, MEDIUM, or LONG) is present in the display, it may be deleted by depressing the corresponding pushbutton switch. The Receiver is now in the manual mode with the gain control under the front panel IF GAIN control. When the Receiver is switched out of the manual mode, it will automatically enter the SHORT AGC mode. The medium or long AGC modes may be selected by depressing the corresponding pushbutton switches. The AGC mode with a manually set threshold is enabled by depressing an AGC mode push-button switch while in the manual mode. The MAN pushbutton switch is the push-on/push-off type. In the manual mode, the AGC pushbutton switches are push-on/push-off, while in the automatic mode they are push-on.

3.2.8 Righthand Keypad Pushbutton Switches

a. TUNE RATE

Provides for fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments) selection of receiver operating frequency through rotation of the Manual Tuning Knob.

b. Numerical Frequency Digit Pushbutton Switches 0 through 9 and ENTER

These are used to set the Receiver to a particular operating frequency. Depressing the ENTER pushbutton switch will enable the numeric keys. The first numeric key depressed will be recognized by the Receiver as the ten's MHz digit. Since the Receiver cannot be tuned above 29.999999 MHz, the Receiver will recognize only 0, 1, or 2 as the first digit entered. The second numeric key depressed will be recognized as the units' MHz digit with the third numeric key depressed as the hundreds' kHz digit.

c. LOCK

This pushbutton switch is the push-on type. When the lock mode is activated, as indicated by the word LOCK in the display, the front panel tuning knob will be disabled. The lock mode is disabled by depressing the TUNE RATE pushbutton switch.

d. BFO, BFO CENTER

These are enabled only if the Receiver is operated in the CW mode. Depressing the BFO will permit selection of the BFO frequency through the front-panel tuning knob. Depressing the BFO CENTER will set the BFO to zero. Depressing BFO CENTER a second time will return the BFO to the previously selected frequency.

e. LOCAL REMOTE

This push-on/push-off type pushbutton switch will set the Receiver to operate either in the LOCAL operating condition (control of the Receiver is through front panel) or the REMOTE operating condition. Note that the Receiver must be equipped with the optional A6A1 Remote Control Interface Circuit Card Assembly to be operated in the remote control condition.

3.2.9 Left (Mode/Meter) Liquid Crystal Display (LCD)

a. −10 0 +10 AF
0 2 4 6 8 10 12 RF

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Located in the upper left corner of the Mode/Meter LCD, the meter display indicates audio level in dBm (when AF selected), and RF in μV (when RF selected). The scale is selected through the METER RF/AF pushbutton switch.

b. BW kHz

Located in the upper right corner of the Mode/Meter LCD, the BW kHz display indicates the IF bandwidth selected through depressing BW1 to BW5 pushbuttons switches.

c. AGC
MAN
SHORT
MEDIUM
LONG

Located in the lower left corner of the Mode/Meter LCD, the word AGC is always present. The word MAN will be present when the Receiver is being operated in the manual gain control mode. Under the word AGC, the words SHORT, MEDIUM or LONG when displayed indicate the type of automatic gain control being used by the Receiver. If both the words MAN and either SHORT, MEDIUM or LONG are present under the word AGC in the display, the Receiver is being operated in an automatic gain control mode with a manually set threshold.

d. MODE
AM
CW
USB
LSB
I-USB
I-LSB
FM
AUX

Located in the middle of the Mode/Meter LCD, the word MODE is always present. The words AM, CW, USB, LSB, I-USB, I-LSB and FM indicate the detection mode of the Receiver. The word AUX is an operator initiated forced bandwidth set-up which is discussed in greater detail in Section V, Maintenance, of this instruction manual.

NOTE

The I-USB and I-LSB functions can only be activated if the ISB option (A5) is installed.

e. TUNING
FAST
SLOW
LOCK
BFO
REMOTE

Located in the lower right corner of the Mode/Meter LCD, the word TUNING is always present. The words FAST and SLOW, when displayed, indicate the rate of frequency change per revolution of the manual tuning knob (refer to Paragraph 3.2.8). The word

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LOCK, when displayed, indicates that the manual tuning knob is disabled. When the words FAST, SLOW and LOCK are not displayed, the Receiver is in the "fine" tuning mode. If the word BFO is present on the display, the manual tuning knob may be used to vary the BFO frequency but will not change the receiver frequency. The word REMOTE is displayed under two conditions: (1) control of the Receiver is under a remote device (provided the Receiver is equipped with the optional A6A1 circuit assembly) and (2) the Receiver is executing a BITE test routine whether under LOCAL control or initiated remotely.

3.2.10 Right (Frequency Data) Liquid Crystal Display (LCD)

a. FREQUENCY MHz

Indicates the tuned frequency, in MHz, of the Receiver. Additionally, during a BITE test sequence routine, a two-digit numerical error code will be displayed if BITE encounters any failed test. (Refer to Section V, Maintenance.)

b. BFO kHz

Indicates selected BFO frequency in kHz with plus or minus sign to indicate direction of offset from IF frequency. When in the CW mode and BFO CENTER is activated, the display shows a single zero.

3.2.11 FAULT Indicator (LED)

A red Light Emitting Diode (LED) indicator lamp will be illuminated if there is a failure in the first, second or BFO frequency synthesizers.

3.3 OPERATING INSTRUCTIONS

The RA6790/GM HF Receiver is internally controlled by a microcomputer which measures and controls many more functions than previously available Receivers. Actual control of the Receiver's parameters is performed by control software contained in Eraseable Programmable Read-Only Memory (EPROMs) within the Receiver. Additionally, a self-diagnostic feature (inclusion of Built-In-Test-Equipment, BITE) allows the Receiver to perform self-test upon command for both local (operator) and remote (computer) control, and report back status data through the addition of data communications capability. While this may increase internal circuit complexity somewhat, actual operating procedures become more simplified.

Additionally, the operator is able to further test the Receiver after BITE has finished its analysis by depressing the appropriate pushbutton switches and observing selected Liquid Crystal Displays (LCDs) on the receiver front panel. The operator can also verify proper operation by performing options and system connections checks, tuning to local AM broadcasts, observing the signal strength meter, and monitoring the audio from the Receiver.

Operation of the remote control module is verified by transmitting and receiving responses with a remote device.

Before attempting to operate the Receiver, it is recommended that: (1) verification of all options and systems connections installation be made in accordance with the procedures detailed in Section II of this manual; (2) the Option Installation Check and System Interface Checks have been performed as presented in Paragraphs 3.3.1 and 3.3.2 of this section; and (3) a thorough review of the front-panel controls and indicators described in Paragraphs 3.1 through 3.2.11 of this section has been accomplished.

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3.3.1 RA6790/GM Receiver Options Installation Check

The purpose of the Options Installation Check is to verify proper Receiver operation after options have been installed, and before the Receiver has been physically installed in its operating location. The check is divided into three parts:

a. IF Bandwidth Filter Installation Check

b. Remote Interface Option Check

c. ISB Option Check

Perform the check(s) appropriate to the configuration of the Receiver being tested. Prior to performing these checks, ensure that:

(1) The Receiver is connected to a suitable power source, and that the pc wafer and fuse match the available line voltage in accordance with Section II, Paragraph 2.3.4.1.

(2) The Receiver is energized (accomplished by switching the POWER ON switch to the ON position; observing that edgelighting is present; and observing that some data is displayed in the MODE and FREQUENCY LCD's).

NOTE

If the Receiver fails to energize, check the power source, fuse, and/or Section V of this manual.

(3) The Receiver is in the LOCAL operating condition which is accomplished by observing the MODE LCD to determine if the word REMOTE is present. If the word REMOTE is not present in the display, proceed with the desired checks. If it is present, momentarily depress and then release the LOCAL/REMOTE pushbutton switch on the righthand keypad. This should remove the word REMOTE from the display and place the Receiver in the LOCAL operating condition.

NOTE

If unable to establish the LOCAL operating condition refer to Section V of this manual.

3.3.1.1 IF Bandwidth Filter Installation Check

This check is used to verify that the proper IF Bandwidth (plug-in type) filters have been installed in the Receiver, and that the filters are functioning properly. To perform this check:

a. Ensure that the preliminary steps listed in Paragraph 3.3.1 have been performed.

b. Ensure that the IF Bandwidth Filters have been installed in accordance with Section II. Paragraph 2.3.3.1.

c. Note the number displayed in the Frequency LCD and write them down.

d. Depress and hold the LOCK pushbutton switch on the righthand keypad.

e. While depressing the LOCK pushbutton, depress the AM pushbutton switch on the lefthand keypad.

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f. Release both pushbuttons.

g. Observe the FREQUENCY MHz LCD. Digits in the display should be rapidly changing, and should continue to change for approximately one minute. If, during this period, the display should stop changing and display a two-digit number, there is a problem with either the filters or with the Receiver itself. Should this condition exist, refer to Section V of this manual. If the numbers stop changing after the one-minute period and return to the numbers noted in step c, the IF Bandwidth Filters are installed correctly.

h. Momentarily depress and then release the AM pushbutton switch on the lefthand keypad. The word AM should be displayed under the word MODE in the Mode LCD.

i. Momentarily depress and then release the BW1 pushbutton switch on the lefthand keypad. Note the number displayed to the left of the word BW kHz in the upper right center of the MODE LCD. This number should approximate ±25% the bandwidth value of the narrowest filter installed. (NOTE: LSB or USB filters excepted, if installed.) The LSB and USB filters can be recognized by the part number stamped on the top of the filter as follows:

LSB filter, 2700 Hz: part number 08409.
USB filter, 2700 Hz: part number 08410.

j. Repeat step i for pushbutton switches BW2 through BW5. The displayed value for BW2 should approximate the bandwidth value of the second narrowest filter; BW3 the third; etc. (NOTE: the number of filters installed dictates the number of active BW switches.) If one or more filter slots (FL1 through FL7 on the A4 module) are empty, one or more BW switches (starting with A5 and working down) will be inactive. The BW switch number (BW1 through BW5) does not necessarily correspond to the FL position number (FL1 thorugh FL7).

k. If, in steps i and j, the bandwidths displayed nearly match the bandwidth values of the installed filters, the filters are functioning properly. If one or more filters do not match the displayed values, replace the filter(s) in question in accordance with Section II, Paragraph 2.3.3.1, and repeat steps i and j until the values do match.

l. Record the value of the filter installed in each slot for future reference. This completes the IF Bandwidth Filter Installation Check.

3.3.1.2 Remote Interface Option Check (Serial Asynchronous Interface)

The purpose of the Remote Interface Option Check is to verify the proper operation of the A6A1 assembly. To perform this check:

a. Ensure that the preliminary procedures outlined in paragraph 3.3.1 have been performed.

b. Connect a suitable remote controller, with its connector wired in accordance with, Section II, Paragraph 2.3.4.6, to the A6A1W1J1 connector on the receiver rear panel.

c. Energize the remote controller and "ask" the Receiver to send its operating parameters to the controller for display. Refer to Paragraph 3.3.3.2 Remote Control Operation. The ASCII command string for this request is:

$99GCR

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where:

S99 addresses receiver number 99 (use the number required for addressing the receiver undergoing test),

G is a "GET" command asking for operating parameters,

CR is "Carriage Return."

d. Note the remote controller display. If any operating parameter information has been displayed at all, the remote interface is working properly. If no data is returned or displayed, refer to Section V of this manual and replace the A6A1 module if required. (Refer to Section II. Paragraph 2.3.3.2 for installation procedure.) This completes the Remote Interface Option Check.

3.3.1.3 ISB Option Check

The purpose of the ISB Option Check is to verify the proper operation of the A5 ISB and the ISB/SSB link on the A4 Main IF module. To perform the ISB Option Check:

a. Ensure that the preliminary procedures outlined in Paragraph 3.3.1 have been performed.

b. Refer to Section II, Paragraph 2.3.3.4 step 2 and set the I-LSB line level. If the line level can be set, the IF portion of the A5 module and the ISB/SSB link are functioning properly. If the line level cannot be set (no signal indication or low signal indication), replace the A5 module. (Refer to Section II, Paragraph 2.3.3.3 for installation procedures.)

c. Connect a headset to the PHONES jack on the receiver front panel and adjust the AF GAIN potentiometer until a signal is heard. If a signal can be heard, the audio portion of the A5 module is operating properly. If no signal is heard, replace the A5 module.

d. If both steps b and c produce satisfactory results, the A5 ISB option is fully operational. This completes the ISB Option Check.

3.3.2 RA6790/GM Receiver/System Interface Check

The purpose of this check is to verify proper operation of the receiving system once the Receiver is installed in its operating location. Prior to performing this check, ensure that the Receiver Options Installation Check(s) outlined in Paragraph 3.3.1 have been completed. To perform the Receiver/System Interface Check:

a. Physically install the Receiver in its operating location.

b. Connect the system RF signal source (antenna; output from multicoupler. etc.) to the RF IN jack J1 on the receiver rear panel.

c. Connect the system remote control device (if used) to connector A6A1W1J1 on the receiver rear panel.

d. Connect the system audio line to the AF OUT connector J3 on the receiver rear panel.

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e. Connect the system external reference frequency source (if used) to REF IN/OUT connector J7 on the receiver rear panel and set the INT/EXT REF switch S2 to EXT.

NOTE

If the Receiver's internal reference is to be used, connector J7 is not used and S2 is set to INT.

f. If the Receiver IF is to be sampled for system use, connect the sampling cable to IF connector J2 on the receiver panel.

NOTE

If the IF is not to be sampled, connector J2 is not used.

g. Connect a suitable ground wire to the GROUND terminal on the receiver rear panel.

h. Connect a headset or plug-in speaker to the PHONES jack on the receiver front panel.

i. Connect the Receiver to a suitable power source by connecting the power line cord to the A10J1 assembly on the receiver rear panel.

CAUTION

Ensure that the voltage value printed on the pc wafer in the A10J1 assembly matches the available line voltage as outlined in Section II. Paragraph 2.3.4.1. Failure to match the Receiver to the available line voltage may result in blown fuses and/or receiver errors.

j. Energize the Receiver by switching the POWER ON switch on the receiver front panel to the ON position.

k. Observe the Mode LCD. The word REMOTE should not be present. If the word REMOTE appears in the display, momentarily depress and then release the LOCAL/REMOTE pushbutton switch on the righthand keypad. The word REMOTE should disappear. If it does not, refer to Section V of this manual.

l. Initialize the Receiver. (Refer to Paragraph 3.3.1 for initialization procedures.) The Receiver will initialize itself in approximately one minute. If after initialization, only a two digit number is displayed in the frequency LCD, and the word REMOTE remains in the Mode LCD, refer to Section V of this manual.

m. Energize (as required) the remaining equipment in the system.

n. Tune the Receiver to a known signal such as a local AM radio station (refer to Paragraph 3.3.3.1 for tuning procedures) and optimize reception so that the signal is clear and intelligible in the headset or speaker. If no signal is heard, try a different signal. If the signal still cannot be heard, check the antenna, multicoupler (if used), antenna cables, RF IN connector, etc. If still no signal is heard, refer to Section V of this manual.

o. Verify that the AF output from the Receiver is present and is being processed by the system AF analysis equipment.

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p. Verify that the IF output (if used) is present and is being processed by the system IF sampling equipment.

NOTE

If either the IF (if used) or AF signals are not present at the input to the analysis equipment, check the appropriate cables and/or connectors. (Especially verify the wiring of mating connector for J3 AF OUT on the receiver rear panel.

q. Using the remote controller, manipulate receiver functions. (Refer to Paragraph 3.3.3.2 for remote control operation.) If the Receiver does not respond to commands from the remote controller, check cables and connections, especially the mating connector for A6A1W1J1 on the receiver rear panel.

Once satisfactory results have been obtained in steps j through q, the Receiver System Interface Check is complete and the system is operational.

3.3.3 LOCAL/REMOTE Control Selection

There are two possible control conditions for operation of the RA6790/GM HF Receiver. In the first or LOCAL control condition, the receiver functions are controlled by selecting modes, levels, bandwidths, etc., using controls physically mounted on the Receiver itself. In the second or REMOTE control condition, the functions are selected by using a coded message sent by a remote operating terminal. It should be noted that when the Receiver is placed in the REMOTE condition, the controls on the Receiver itself are non-functional. Determination of which condition the Receiver is in (i.e. LOCAL or REMOTE) can be made simply by checking the lower-right corner of the receiver's mode LCD. If the Receiver is in REMOTE, the word REMOTE will be displayed. If the Receiver is in LOCAL, no word will be displayed. Switching between the two conditions is achieved by pressing and releasing the LOCAL/REMOTE pushbutton switch on the righthand keypad.

3.3.3.1 LOCAL Control Operation

The following procedures are to be used to operate the RA6790/GM HF Receiver in the LOCAL control condition:

a. Ensure that all desired options have been installed and that the Receiver Options Installation Check has been performed in accordance with Paragraph 3.3.1.

b. Turn POWER ON switch to ON position. Indications that the Receiver is energized include:

(1) Edgelight illuminated.

(2) Some data shown in Liquid Crystal Displays (LCD's).

(3) Sounds in audio device (headphones or speaker). If Receiver does not energize when POWER switch is toggled, refer to Section V of this manual.

c. Establish LOCAL control. Momentarily depress the LOCAL/REMOTE pushbutton switch on the righthand keypad while observing the lower-right corner of the mode LCD. Depress the switch again. Note that the display will show the word REMOTE on alternate pressings of the switch, while REMOTE disappears on alternate pressings.

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When the Receiver is under LOCAL control, the word REMOTE is not shown in the display. If the word REMOTE cannot be alternately displayed and erased, refer to Section V of this manual.

d. Initialize the Receiver. The RA6790/GM Receiver has a built-in capability to self-determine the values of the IF bandwidth filters installed, and to assign these filters to particular bandwidth pushbuttons (BW1 through BW5 on the lefthand keypad). These bandwidth assignments normally result in the narrowest bandwidth filter being assigned to the BW1 pushbutton with increasingly wider bandwidths being assigned to BW2, BW3, etc. in ascending order. This assignment process is done as a part of receiver initialization. (The remainder of the initialization process is a series of Built-In-Test-Equipment (BITE) checks which are addressed in Section V. Do not be concerned with BITE at this time.)

To initialize the Receiver:

(1) Press and hold the LOCK pushbutton switch on the righthand keypad.

(2) While holding down the LOCK pushbutton, press the AM pushbutton switch on the lefthand keypad.

(3) Release both the LOCK and AM pushbuttons simultaneously. The normal indications that the Receiver is in the initialization process are:

(a) The word REMOTE will appear in the Mode LCD.

(b) The frequency LCD will begin displaying a series of rapidly changing digits in both the FREQUENCY and BFO portions of the display.

(c) Rapidly changing sounds and tones in the audio device (speaker or headset).

(d) Changing modes and levels in the mode LCD.

Indication that the initialization process is complete is obtained by observing the word REMOTE in the mode LCD. When REMOTE is erased and the Receiver returns to the displayed values that were present prior to the initialization process, the process is complete. (NOTE: The Initialization process takes approximately one minute to complete.) If during the process the display stops changing and a two-digit number appears and remains in the FREQUENCY LCD, BITE has detected a problem in the Receiver. Refer to Section V of this manual.

e. Select Desired Frequency (00.500000 MHz to 29.999999 MHz). There are two methods for selecting any desired frequency. The first of these is to enter the frequency digits directly using the ENTER pushbutton switch and the numeral pushbutton switches on the righthand keypad. The second is to select a tune rate and manually tune to the desired frequency using the manual tuning knob. The procedures for each of these methods are as follows:

(1) Direct Entry:

(a) Momentarily depress and release the ENTER pushbutton switch on the righthand keypad.

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(b) Starting with the lefthand digit of the desired frequency, momentarily depress then release the corresponding numeral pushbutton switch on the righthand keypad.

NOTE

Frequencies less than 10.0000 MHz require an initial zero (0) digit entry. The decimal point will automatically appear in the display without a decimal point entry from the operator.

EXAMPLE 1:
Desired Frequency: 14.2514 MHz
Keystrokes Required:

ENTER
1
4
2
5
1
4
0
0

Resulting Display in FREQUENCY LCD: 14.251400

EXAMPLE 2:
Desired Frequency: 3.75 MHz
Keystrokes Required:

ENTER
0
3
7
5
0
0
0
0

Resulting Display in FREQUENCY LCD: 03.750000

EXAMPLE 3:
Desired Frequency: 0.57 MHz
Keystrokes Required:

ENTER
0
0
5
7
0
0
0
0

Resulting Display in FREQUENCY LCD: 00.570000.

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(2) Manual Tuning:

Ensure that the word LOCK is not present in the mode LCD. If it is present, momentarily depress then release the TUNE RATE pushbutton switch on the righthand keypad. The word LOCK should disappear. If LOCK cannot be removed from the display, refer to Section V of this manual.

f. Select Tune Rate. This is accomplished by alternate depressions of the TUNE RATE pushbutton switch. Observe the right side of the Mode LCD. One of three displays should be present under the word TUNING: SLOW, FAST, or no display (refer to Paragraph 3.2.9). These three displays correspond to three rates of change of frequency caused by rotation of the Manual Tuning Knob as follows:

No display: Fine tuning, small incremental change as knob is rotated.
SLOW: Slow tuning, faster than fine tuning.
FAST: Fast tuning, largest incremental change per knob rotation.

Rotate Manual Tuning Knob to desired frequency changing tune rates as desired.

EXAMPLE:
Receiver is set at 20.179000 MHz, and the desired frequency is 10.853000 MHz.

(1) Select FAST tune rate.

(2) Tune to approximately 10.8 MHz, using manual tuning knob.

(3) Select SLOW tune rate.

(4) Tune to approximately 10.85 MHz using Manual Tuning Knob.

(5) Select fine tuning rate.

(6) Tune to 10.853000 MHz using Manual Tuning Knob.

g. Select Detection Mode. (AM, CW, USB, LSB, ISB U/L, FM). Detection modes are selected by momentarily depressing and then releasing the appropriate pushbutton switch on the lefthand keypad. A discussion of operation in each mode follows.

h. AM.

(1) Depress and release the AM pushbutton switch. Indications that the Receiver is in the AM mode are: the word AM under MODE in the Mode LCD; a one or two digit number next to BW KHZ in the upper right corner of the Mode LCD.

If unable to achieve these indications, refer to Section V of this manual.

(2) Select desired IF bandwidth (BW1 through BW5). IF bandwidths range from narrowest (BW1) to widest (BW5), with values of the IF bandwidth filters actually installed in the Receiver. To select a bandwidth, depress and release one of the bandwidth selection pushbutton switches (BW1 through BW5). The bandwidth of the filter selected will appear next to the BW KHZ words in the mode LCD. If no number appears for a particular bandwidth then either no filter has been installed for that position or there is a problem with the Receiver.

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NOTE

If a full complement of filters (7) has been installed and a no-number bandwidth appears, re-initialize the Receiver. If the condition persists, refer to Section V of this manual. If less than a full complement of filters (less than 7) has been installed, the no-number condition on one or more bandwidths is normal and should be disregarded except to ensure that, for operating, a bandwidth with a number displayed must be selected.

(3) Select Gain Control (AGC, MAN, SHORT, MED, LONG). There are three choices for IF Gain Control:

(a) Automatic (AGC)

(b) Manual

(c) Automatic with Manual Threshold

A discussion of these choices follows.

i. Automatic (AGC). AGC automatically establishes and maintains a desirable IF signal level. Through the use of operator selectable response times, it also establishes the time it takes for the AGC circuitry to respond to IF signal level changes. To select AGC:

(1) Observe the mode LCD under the word AGC. If the word MAN is displayed, momentarily press and release the MAN pushbutton switch on the lefthand keypad. the word MAN should disappear. In addition, another word (LONG, MED, or SHORT) should be displayed under AGC on the display.

(2) Select the response time by depressing and releasing the desired pushbutton switch (LONG, MED, or SHORT) on the lefthand keypad. The Receiver is now under automatic gain control.

j. Manual. Manual gain control allows the operator to set a desired IF signal level, and disables the automatic response and adjustments to changes in IF signal level. To select manual gain control:

(1) If the word MAN is not present under the word AGC on the Mode LCD, momentarily depress and release the MAN pushbutton switch on the lefthand keypad. The word MAN will appear on the display.

(2) If under the word MAN another word (LONG, MED, or SHORT) is present, momentarily depress and release the pushbutton switch on the lefthand keypad which corresponds to the displayed word. Once the word MAN is the only displayed word under AGC on the mode LCD, the Receiver is under manual gain control.

(3) Observe the level meter display in the upper left corner of the Mode LCD. If the word RF is displayed proceed to (4). If the word AF is displayed, momentarily depress and release the METER RF/AF pushbuttons switch on the lefthand keypad to change the display to RF.

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(4) Once RF is displayed in the mode LCD and the Receiver is under manual gain control, the IF GAIN potentiometer may be adjusted to the desired signal level by rotating the knob while observing the RF level indication on the meter in the mode LCD.

k. AGC with Manual Threshold. This gain control capability allows the operator to manually set the desired IF signal level which the AGC automatically maintains. Response times are operator selectable through the LONG, MED or SHORT pushbutton switches on the lefthand keypad. To select AGC with manual threshold:

(1) Select manual IF gain control as directed in j.

(2) Set desired signal level as desired according to j (4).

(3) Momentarily depress and release the desired response time pushbutton switch (LONG, MED or SHORT) on the lefthand keypad.

The Receiver is now under AGC with manual threshold control. Indications that the Receiver is in this condition are:

(a) The word MAN is displayed under the word AGC in the mode LCD.

(b) The word LONG, MED or SHORT is displayed under the word MAN in the mode LCD.

l. CW. Select the CW mode by depressing and releasing the CW pushbutton switch. Indications that the Receiver is in the CW mode are:

(a) The word CW under MODE in the mode LCD.

(b) The appearance of digits under BFO KHZ on the FREQUENCY LCD.

Select BFO (Beat Frequency Oscillator) Frequency (–8.0, 0, +8.0 kHz). The BFO may be operated in either of two conditions:

(a) BFO - adjustable

(b) BFO CENTER - non-adjustable

NOTE

BFO functions can be controlled by the operator only in the CW mode, and are disconnected from their controls in all other modes.

m. The BFO condition allows the operator to tune the BFO manually to achieve the desired audio frequency for received CW signals. The BFO CENTER condition allows the operator to zero-beat (fine tune the Receiver to the exact RF) the incoming CW signal. To select BFO Frequency (adjustable):

(1) Observe the BFO kHz portion of the FREQUENCY LCD. If a three digit number and a "+" or " – " sign is displayed proceed to step 2. If a single zero preceeded by a " + " sign is displayed, momentarily depress and release the BFO CENTER

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pushbutton switch on the righthand keypad. This should cause the display to show a three digit number preceeded by either a " + " or " – " sign.

(2) Observe the mode LCD and note the display under the word TUNING. If the word BFO is displayed, proceed to step 3. If there is no word displayed under tuning, or if SLOW, FAST, or LOCK is displayed, momentarily depress and then release the BFO pushbutton switch on the righthand keypad. The word BFO should now be displayed under the word TUNING on the mode LCD.

(3) Rotate the manual tuning knob while observing the BFO KHZ portion of the FREQUENCY LCD. The numbers displayed should change as the knob is rotated.

(4) Select the desired BFO Frequency (+8.0 kHz to –8.0 kHz) either by watching the BFO KHZ display while rotating the knob until the desired BFO Frequency is attained, or by listening to the audio signal while rotating the knob until the desired audio frequency is heard.

To select BFO CENTER (for zero-beating the incoming signal):

(1) Observe the BFO KHZ portion of the frequency LCD. If a single zero preceeded by a " + " sign is displayed, proceed to step (2). If a three digit number preceeded by a " + " sign is displayed, momentarily press and then release the BFO CENTER pushbutton switch on the righthand keypad. A single zero preceeded by a "+ " sign should now be displayed.

(2) Observe the mode LCD and look under the word TUNING. If there is no word displayed under TUNING or if SLOW or FAST are displayed, proceed to step (3). If either the word LOCK or the word BFO is displayed, momentarily depress and then release the TUNE RATE pushbutton switch on the righthand keypad. The word LOCK or BFO should disappear.

(3) The incoming signal may now be fine-tuned by slowly rotating the manual tuning knob until the audio tone from the signal is nulled.

(4) Momentarily depress and then release the BFO CENTER pushbutton switch and observe that a three digit number preceeded by a " + " or " – " sign appears in the BFO KHZ portion of the FREQUENCY LCD.

(5) Momentarily depress and then release the BFO pushbutton switch on the righthand keypad. The word BFO should appear in the mode LCD.

(6) Slowly rotate the manual tuning knob until the desired BFO Frequency is obtained.

(7) Momentarily depress and then release the LOCK pushbutton switch on the righthand keypad. This disables both the manual tuning and BFO adjustment functions preventing loss of the signal if the manual tuning knob is inadvertently rotated.

(8) Select IF bandwidth as outlined in h. (2).

(9) Select gain control as outlined in h. (3).

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o. USB or LSB

(1) Select either upper sideband or lower sideband mode by momentarily depressing and then releasing the appropriate (USB or LSB) push-button switch on the lefthand keypad. Either USB or LSB should appear under the word MODE on the mode LCD.

(2) All other functions in USB or LSB are identical to the AM mode (except for IF bandwidth, which is fixed in either the USB or LSB mode).

p. ISB U/L (available only if ISB option A5 assembly is installed).

(1) Select the independent sideband mode by momentarily depressing and then releasing the ISB U/L pushbutton switch on the lefthand keypad. The word I-USB or I-LSB should appear under the word MODE on the mode LCD. Subsequent depressing and releasing of the ISB U/L pushbutton will alternately display I-USB or I-LSB.

NOTE

If the ISB option is not installed, depressing the ISB U/L pushbutton switch will have no effect on receiver operation.

(2) Other functions are identical to those of the AM mode.

NOTE

Each sideband is independently controlled in this mode. Therefore separate AGC settings are possible for both I-USB and I-LSB.

q. FM.

(1) Select the FM mode by momentarily depressing and then releasing the FM pushbutton switch on the lefthand keypad. The word FM will appear under the word MODE in the mode LCD.

(2) Other functions are identical to those of the AM mode.

r. Forced IF Bandpass Filter Bandwidth Setup

In case BITE results are unsatisfactory, the forced IF bandpass filter bandwidth setup can be initialized by simultaneously depressing the LOCK and ISB U/L pushbutton switches, and observing the AUX indicator displayed in the MODE LCD. This process accesses RAM within the microprocessor circuit card assembly (A6A2) for loading of the IF bandpass filter bandwidth complement. It should be noted, however, that this setup cannot be accomplished during the BITE routine. In addition, the setup can be terminated (if desired) before all seven filter slots FL1-FL7 have been changed, and when all seven filter slots have been loaded, the AUX indicator will go off (disappear) automatically, thus, disabling any further changes and resetting the receiver to normal operation.

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(1) Symmetrical Filter Entry

NOTE

Entry of symmetrical filters is accomplished using the 0-9 numeral pushbutton switches, in 100 Hz steps, delimited with the ENTER pushbutton switch. For example, to enter a .4 kHz (400 Hz) filter, the "4" and "ENTER" pushbutton switches would be depressed; to enter 20 kHz, the "2", "0", "0", "ENTER" pushbutton switches would be depressed (200 x 100 Hz = 20 kHz).

(a) Depress and release the appropriate numeral pushbutton switches (0-9) on the right-hand keypad, then depress and release ENTER pushbutton switch.

NOTE

In the case of blank filter slots, load by depressing the ENTER pushbutton switch only.

(2) USB and LSB Filter Entry

(a) Depress and release USB and/or LSB pushbutton switch(s) on the left-hand keypad, and observe AUX indicator displayed go off in the MODE LCD.

NOTE

In the case of blank filter slots, load by depressing the ENTER pushbutton switch only.

(3) Terminating Forced IF Bandpass Filter Bandwidth Setup:

(a) Depress and release ISB U/L pushbutton switch on the left-hand keypad, and observe AUX indicator displayed go off in the MODE LCD.

3.3.3.2 REMOTE Control Operation (Serial Asynchronous Interface)

If the Receiver is equipped with the optional A6A1 remote control interface assembly, the Receiver may be operated by a remote-control device. Before attempting to operate the Receiver in the remote operating condition, it is recommended that the operator be thoroughly familiar with operating the Receiver in the local operating condition (refer to Section III, Paragraphs 3.3.3 and 3.3.3.1). "Hands-on" experience working with the Receiver in the local operating condition provides the operator with a working knowledge of receiver capabilities, signal optimization, and control interaction. Such knowledge is essential to obtaining satisfactory results when controlling the Receiver from a remote location.

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The minimum considerations when discussing RA6790/GM HF Receiver remote operation are:

(1) Remote Control Data Character

(2) Remote Control Device

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(3) Input/Output Electrical Interface

(4) Remote Control Commands

(5) RA6790/GM HF Receiver responses to remote control commands.

(6) Functions unique to the remote control operating condition.

Each of these considerations is addressed in a following paragraph.

a. Remote Control Data Character.

The data character used for remote control is the standard ASCII asynchronous format which consists of a start bit, seven data bits (one ASCII Character), a parity bit, and two stop bits. Figure 3-1 shows the data character format, and Table 3-1 lists standard ASCII character codes.

b. Remote Control Device.

Any remote-control device (terminal, receiver control panel, etc.) which generates and accepts the standard ASCII asynchronous format may be used to control the Receiver.

NOTE

Due to the wide variety of possible control devices, the discussion on remote control commands addresses ASCII characters rather than on specific control pushbuttons, keys, or switches. Similarly, the discussion on RA6790/GM HF Receiver responses to remote-control commands addresses the ASCII characters sent back to the controller, rather than on specific displays generated by the receipt of those responses.

c. Input/Output Electrical Interface.

The input/output electrical interface consists of the A6A1 serial asynchronous interface assembly which connects to the remote control device through the A6A1W1J1 Connector (type M83723-02R-1626N) on the receiver rear panel. The interface, which provides separate lines for command input and monitor output data, allows up to ten (10) Receivers to be placed on a common, parallel, input/output bus. The command receiver meets the specifications of RS423, RS422 and MIL-STD-188-114, and is also operable with MIL-STD-188C or RS232 compatible remote control devices. The monitor transmitter meets the specifications of RS423 and MIL-STD-188-114, and is operable with MIL-STD-188C or RS232 compatible devices and may be strapped for RS422 unipolar operation. Interface selection, receiver address baud rate selection, and parity odd/even selection wiring instructions are discussed in Section II, Paragraphs 2.3.3.2 and 2.3.4.6.

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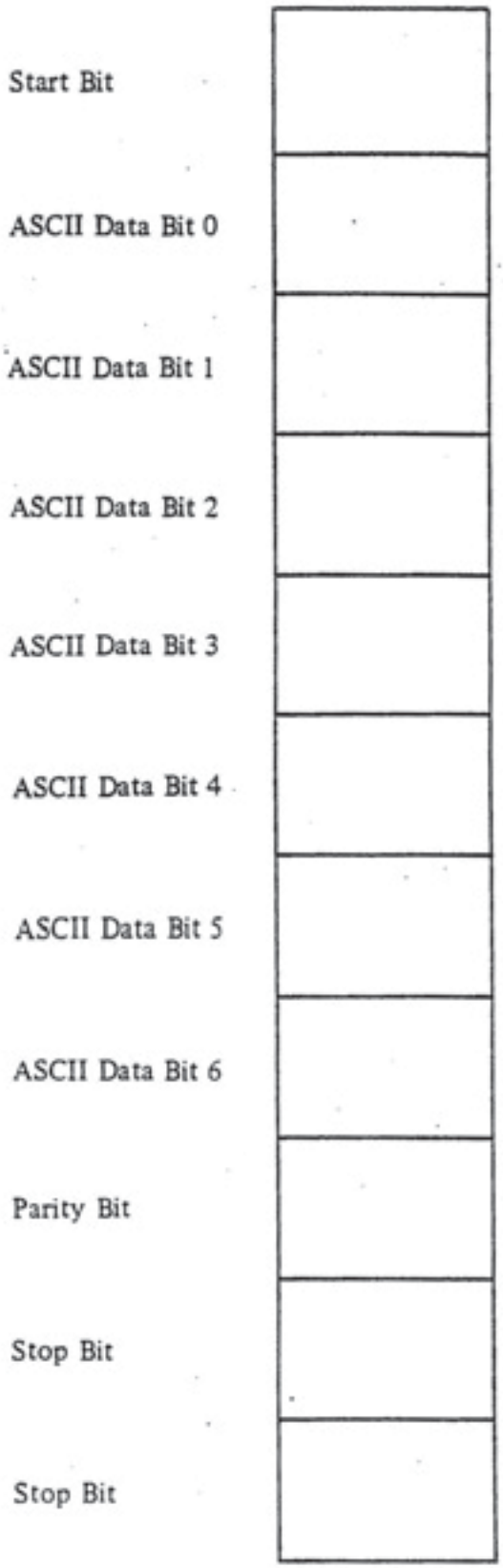

Figure 3-3. Data Character Format

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TABLE 3-1. ASCII CHARACTER CODES

ASCII Character	Octal Code	Decimal Code	ASCII Character	Octal Code	Decimal Code
NUL	00	0	SP	40	32
SOH	01	1	!	41	33
STX	02	2	"	42	34
ETX	03	3	#	43	35
ETO	04	4	$	44	36
ENQ	05	5	%	45	37
ACK	06	6	&	46	38
BEL	07	7	'	47	39
BS	10	8	(	50	40
HT	11	9	)	51	41
LF	12	10	*	52	42
VT	13	11	+	53	43
FF	14	12	,	54	44
CR	15	13	-	55	45
SO	16	14	.	56	46
SI	17	15	/	57	47
DLE	20	16	Ø	60	48
DC1	21	17	1	61	49
DC2	22	18	2	62	50
DC3	23	19	3	63	51
DC4	24	20	4	64	52
NAK	25	21	5	65	53
SYN	26	22	6	66	54
ETB	27	23	7	67	55
CAN	30	24	8	70	56
EM	31	25	9	71	57
SUB	32	26	:	72	58
ESC	33	27	;	73	59
FS	34	28	<	74	60
GS	35	29	=	75	61
RS	36	30	>	76	62
US	37	31	?	77	63

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TABLE 3-1. ASCII CHARACTER CODES (Cont.)

ASCII Character	Octal Code	Decimal Code	ASCII Character	Octal Code	Decimal Code
@	100	64	(Apost)	140	96
A	101	65	a	141	97
B	102	66	b	142	98
C	103	67	c	143	99
D	104	68	d	144	100
E	105	69	e	145	101
F	106	70	f	146	102
G	107	71	g	147	103
H	110	72	h	150	104
I	111	73	i	151	105
J	112	74	j	152	106
K	113	75	k	153	107
L	114	76	l	154	108
M	115	77	m	155	109
N	116	78	n	156	110
O	117	79	o	157	111
P	120	80	p	160	112
Q	121	81	q	161	113
R	122	82	r	162	114
S	123	83	s	163	115
T	124	84	t	164	116
U	125	85	u	165	117
V	126	86	v	166	118
W	127	87	w	167	119
X	130	88	x	170	120
Y	131	89	y	171	121
Z	132	90	z	172	122
[	133	91	{	173	123
/	134	92	:	174	124
]	135	93	}	175	125
	136	94	~	176	126
–	137	95	DEL	177	127

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d. Remote Control Commands.

If, for example, a Receiver has been designated receiver number 99 and the mating connector for A6A1W1J1 has been wired accordingly, then to remotely control receive number 99, the following command string (ASCII format) must be sent from the remote control device to the Receiver:

$99S2CR

The "$" character alerts all Receivers on the common bus that an address command is coming. "99" alerts receiver number 99 that all subsequent commands, when they come, will be specifically addressed to it until another "$" character is received. "S2" is a status command which tells the Receiver to set itself to the remote operating condition, and "CR" is carriage return which is the final character sent to the Receiver in each command string. (CR is interpreted by the Receiver as an "execute" instruction, and causes the Receiver to carry out all commands in the string; in this case "set up for remote control.")

The other status (S) commands which may be used to follow "$99" are:

S1 Set Receiver to local control
S2 Set Receiver to remote control
S3 Initiate BITE self-test sequence
S4 Terminate BITE self-test sequence
S5 Report bandwidth of installed IF filters
S6 Report BITE results
S7 Forced bandwidth setup (discussed in Section V)
S8 Enable remote AGC dump
S9 Inhibit remote AGC dump

Status commands may be sent to only one Receiver at a time since some of the status commands will result in monitor data being sent back to the remote-control device from the Receiver.

Once the Receiver has been set for remote operation by the "S2" command, the next step normally is to initiate the BITE self-test sequence by sending "S3" (quotation marks are used here for clarity only and are not part of the S3 command). The BITE routine requires approximately one minute to complete. After the BITE routine is complete, the "S6" command will cause the Receiver to report its findings. The "S5" command will then report a list of IF filter bandwidths. These bandwidths should be compared with the Receiver configuration chart to determine if the filters are working properly. If the BITE report displays an error code number, refer to Section V of this manual. Note that once a particular Receiver has been addressed by the "$NS2" command (N is 99 in this case), subsequent commands (S3 or S6 or S5) to the Receiver need not be prefixed by the "$N" (Receiver address). A typical command string normally sent to initiate remote control operation is illustrated in Example 1.

EXAMPLE 1:

1st entry: $99S2CR – Sets receiver 99 for remote control

2nd entry: S3CR – initiates BITE self-test routine in receiver 99

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3rd entry: S6CR - requests BITE routine results from receiver 99

4th entry: S5CR - requests values of IF bandwidth filters found in receiver 99

(Commands "S5" and "S6" will result in data responses from the Receiver to the remote control device.)

5th entry: S7CR - this command is used to force a particular IF bandpass filter bandwidth complement in the receiver. Allowable codes are L for lower sideband (LSB), U for upper sideband (USB), N for none, and bandwidths up to 20 kHz (in kHz) with a resolution of 100 Hz. Symmetrical bandwidths (in kHz) are terminated with a comma. The string may contain all seven IF bandpass filters (FL1-FL7) bandwidths or it may end early with a carriage return (CR). Filter slots not entered will not be altered by the S7 command. A typical command is as follows:

S7LU1.7,.4,N3.2,(LF)

The preceeding command sets up the following:

Filter Slot	Filter/Function
FL1	Lower Sideband (LSB)
FL2	Upper Sideband (USB)
FL3	1.7 kHz (Symmetrical)
FL4	400 Hz (Symmetircal)
FL5	None
FL6	3.2 kHz (Symmetircal)
FL7	Unchanged from previous setting

6th entry: S8CR - this command causes all subsequent commands containing receiver data to cause an automatic AGC dump.

7th entry: S9CR - this command causes the AGC dump to be disabled. This would be used when free tuning the receiver by remote control.

Two additional commands will result in data responses from the Receiver to the remote-control device. The commands are called monitor commands and instruct the Receiver to report certain specified data on receipt of the command. The monitor commands are "G" (for "Group") and "T" (for "Talk").

EXAMPLE 2:

The command $99GCR will result in all of the following data (depending on mode) being sent from receiver 99 to the remote control device in the order indicated.

RF Frequency
Detector Mode
Gain Control Mode
IF Bandwidth
BFO Frequency
IF Attentuation
Status

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(The actual information sent by the Receiver and its format is shown in the discussion on RA6790/GM HF Receiver responses to remote control commands.)

"T" commands result in selected data being sent back to the remote control device.

EXAMPLE 3:

The commands $99 TFCR will result in only frequency and summary status data being sent to the remote control device.

"T" commands include:

TF - requests frequency data only.
TD - requests detector mode data only.
TI - requests IF bandwidth data only (non-functional in ISB mode).
TM - requests IF gain control mode data only.
TB - requests BFO data only (functional only when Receiver is in BFO variable).
TA - requests IF gain control attenuation data only (functional only when Receiver is under manual IF gain control or AGC with manual threshold).

Several "T" commands may be sent to the Receiver at once by listing the desired information characters after only one "T".

EXAMPLE 4:

$99TFDICR would result in frequency detector mode, bandwidth and summary status information being sent back to the remote control device.

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The following commands cause the Receiver to change operating parameters, but do not result in data responses to the remote control device. Therefore, more than one Receiver may be addressed at once by inserting commas (in ASCII format) between the receiver numbers.

EXAMPLE 5:

The command: $99,14,27,F5CR would result in receiver number 99, 14, and 27 being set to a frequency of 05.000000 MHz.

NOTE

Once multiple receivers have been addressed as in this example, two things must be remembered: (1) any subsequent parameter change command preceding the next $ will result in that parameter being changed on all receivers addressed (in the example, receiver numbers 99, 14, and 27); (2) A status or monitor command may not be sent before the next $, since more than one Receiver cannot respond on the bus at the same time. If a status or monitor command is sent, the command is simply ignored. To change only one receiver's operating parameter(s) or to send a status or monitor command, the desired Receiver must be readdressed individually ($99 or $14 or $27 in Example 5).

Frequency Selection. The command is in the format FN where N is used to select the Receiver(s) operating frequency. The frequency command may specify the desired frequency down to 1 Hz. For example, the command F03.415926 would tune the Receiver(s) to 3.415926 MHz. If an exact frequency is not required, the leading and trailing zeros may be eliminated. The command F3.4 would tune the Receiver(s) to 3.400000 MHz. Note that in both cases a decimal point is required to indicate MHz. If an exact multiple of 1 MHz is desired (as in Example 5), "F" followed by the desired MHz number (as in Example 5) may be sent without a decimal point. This will tune the addressed receiver to the exact whole multiple of 1 MHz specified.

Detector Mode Selection. The desired detector mode is selected by sending the command DN where N is the desired detector mode as follows:

D1 – AM
D2 – FM
D3 – CW with variable BFO
D4 – CW with BFO CENTER
D5 – ISB (if ISB option is installed)
D6 – LSB
D7 – USB

BFO Offset. The BFO offset frequency may be set by sending the command BN where N indicates the offset frequency in kHz. For example, the command B+1.82 will set the BFO offset 1.82 kHz above the center frequency; B–4.65 will set the offset 4.65 kHz below the center frequency.

Bandwidth Selection. The desired bandwidth is selected by sending the command IN where N indicates the filter bandwidth in kHz. For example, the command I3.24 would

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select the 3.24 kHz filter. If a command is received that does not match the filter in the Receiver, the Receiver will automatically select the closest filter. For example, the command I7. will select the 6.8 kHz filter. Note that the decimal point is used to indicate kHz.

Gain Control Mode. The desired gain control mode is selected by sending MN where N is the desired gain control mode as follows:

M1	Selects short AGC time constant
M2	Selects medium AGC time constant
M3	Selects long AGC time constant
M4	Selects manual gain control
M5	Selects short AGC with manually set threshold
M6	Selects medium AGC with manually set threshold
M7	Selects long AGC with manually set threshold

Manually Set Gain Control. The Receiver will respond to remote commands to set a manual gain. The receiver IF gain is controlled by adding attenuation (from 0 to a maximum of 120 dB) to the amplifier circuit. This feature may also be used in conjunction with the AGC operation to establish a minimum threshold level for the AGC. The command for setting the level is AN where N represents the approximate amount of attenuation (N X0.8 in dB) to be added to the circuit. For example, the command A3 would add approximately 3 dB of attenuation to the amplifier circuit; A104 would add approximately 80 dB of attenuation.

EXAMPLE 6:

The command: $99F2.35D3I1.5M5A55B-1.7CR would result in receiver number 99 to be set to the following parameters:

Selected Receiver:	99
Frequency:	02.350000 MHz
Detector Mode:	CW with variable BFO
IF Bandwidth:	Closest installed IF bandwidth filter to 1.5 kHz
Gain Control:	Short AGC with manually set threshold
Attenuation:	Threshold of approximately 40 dB
BFO Frequency:	1.70 kHz below center frequency

e. RA6790/GM HF Receiver Responses to Remote Control Commands.

Status commands "S5" and "S6," and monitor commands "G" and "T" request data to be sent from the Receiver to the remote control device. This data is obtained and transmitted when the command (followed by a CR) is sent to any one receiver address. The format of the response depends on the data requested.

"S5" triggers a data stream in the following format:

BW(FL1), BW(FL2), FW(FL3), BW(FL4), BW(FL5), BW(FL6), BW(FL7) where BW is the bandwidth in kilohertz and FL1-FL7 is the filter slot checked.

EXAMPLE 7:

The command $99S5CR might obtain the following response:

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L,U,1.6,.5, ,2.7,16 where

L – Lower sideband filter in filter slot FL1
U – Upper sideband filter in filter slot FL2
1.6 – 1.6 kHz filter in filter slot FL3
.5 – 500 Hz filter in filter slot FL4
, , – No filter in filter slot FL5
2.7 – 2.7 kHz filter in filter slot FL6
16 – 16 kHz filter in filter slot FL7

"S6" triggers a data stream in one of two formats as follows:

:OKNCR, where N is the receiver number and CR is carriage return.

or

:X,Y,Z,ENDNCR, where X, Y, and Z would represent the two digit BITE error codes, N is the receiver number, and CR is carriage return.

EXAMPLE 8:

:OK99 indicates that receiver 99 passed all BITE tests

or

:4,17,33END99 indicates that receiver 99 found BITE error codes 4, 17, and 33. (Refer to Section V for explanation of BITE error codes.)

"G" triggers a data stream in the following format:

F, D, M, I, B, A, S where:

F is receiver frequency in MHz
D is receiver detector mode
M is receiver gain control mode
I is receiver IF bandwidth
B is BFO frequency (only functional in CW variable BFO mode)
A is IF attenuation (only functional with manual gain control or AGC with manual threshold)
S is receiver status

EXAMPLE 9:

The command S99GCR might result in a response such as: F2.35D3M5I1.5B-1.7A55S2 which indicates the following parameters:

Selected Receiver:	99
Frequency:	2.350000 MHz
Detector Mode:	CW with variable BFO
Gain Control:	Short AGC with manual threshold
IF Bandwidth:	1.5 kHz
BFO Frequency:	1.70 kHz below center frequency
Attenuation:	Threshold of ≈40 dB
Status:	Receiver is under remote control

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NOTE

Status responses differ from status commands. Refer to next paragraph.

Status Response. The status data is sent as the last item in each monitor response ("G" or "T") from the Receiver. The status data is returned to the remote-control device in the format SN, where N is a one or two digit number representing the following conditions:

0 Receiver is operating in local control operating condition.
1 Receiver is operating in remote control operating condition.
2 Synthesizer is out of lock.
4 Receiver is in the override mode (discussed under Functions Unique to the Remote Control Operating Condition).
8 Last command sequence had character transmission error.
16 Last command sequence had data error.
32 Lost data error in last sequence.

If two or more conditions are present, the numbers representing the conditions will be added together and transmitted as one number. For example, 17 (1 + 16) would indicate that the Receiver is in remote control and last command sequence had a data error; 13 (8 + 4 + 1) would indicate remote control, override mode and character transmission error. Note that some numbers are not valid, i.e. 12 since override mode is impossible while in LOCAL control.

The next status response to be considered is "TX" where X is the desired parameter(s) which triggers a data stream in the following format:

XVS where:

X is the identity letter of the parameter (F, D, M, I, B, or A)
V is the value of the parameter
S is the status response

EXAMPLE 10:

The command S99TFDCR might obtain a response such as: F2.35D3S1 where:

Frequency:	02.350000 MHz
Detector Mode:	CW with variable BFO
Status:	Receiver is in the remote operating condition

f. Functions Unique to the Remote Operating Condition

Override Mode. The remote control device may be used to command a Receiver to switch to the override mode. In override mode, some of the automatic operating features of the Receiver are disabled. This is, the first local oscillator is always tuned to 40.455 MHz above the entered RF frequency and the IF slot is selected remotely regardless of the type of filter installed. Therefore, the remote controller must decide what the filter should be used for, the type of detection mode to employ, and the BFO offset to receive a signal. For instance, in sideband detection with a symmetrical filter, the first local oscillator and BFO must be properly offset to correctly demodulate the signal. The remote controller also assumes the

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responsibility for ensuring that the filter is installed in the selected slot, since an empty slot will cause a dead receiver. The override mode blanks the display. In addition, override signals cannot be handed off to the operator, since the machine has no way of deciding the difference between a sideband signal with virtual carrier offset or a CW signal with a BFO offset. The override mode is invoked when both detector and bandwidth are sent in the same command with the = sign. Sending either without the equals stores = data but removes the Receiver from the override mode and restores it to normal operation. The Receiver will respond to the following override commands (in the format $ND=XI=Y where N is the receiver number, X is the mode selection number, and Y is the filter slot number):

Mode Selection. The desired mode is selected by sending one of the following commands:

D=1 Selects envelope detector
D=2 Selects continuous-wave detector
D=3 Selects frequency-modulation detector
D=4 Selects ISB operation

Note that these "D" commands differ from the normal "D" commands and are unique to the override mode.

Filter Selection. In the override mode the filters are selected according to the filter slot number instead of the filter bandwidth. The command is I = N where N corresponds to the filter slot number. For example, the command I=3 will select the filter inserted in filter slot FL-3.

EXAMPLE 11:

The command $99D=2I=3CR would result in receiver 99 being set to the override mode using the CW detector and the filter installed in filter slot FL-3.

To exit the override mode, an "IN" command is sent where "N" is the desired bandwidth in kHz (not the filter slot number), and the " = " sign is omitted.

NOTE

When the Receiver is in the override Mode, both the MODE LCD and the FREQUENCY LCD are blanked. In addition, status command S1 will be ignored by the Receiver.

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SECTION IV
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

Section IV describes the theory of operation for the RA6790/GM HF Receiver. The theory traces primary signal flow as it progresses through the various components of the Receiver and details the functional relationships of each component to the signal flow. This section is divided into two main discussions: (1) Functional, detailing, the primary signal flow as related to the Receiver's operation; and (2) a detailed circuit description of each assembly and the components included on each card. Simplified functional block diagrams, timing diagrams and tables are used throughout the text to aid the technician in understanding the theory of operation to the circuit level. (Refer to Figure 4-1.)

4.2 FUNCTIONAL THEORY OF OPERATION

The primary signal from the antenna input, through the Receiver, to the audio output and secondary functions as they are related to that primary signal flow are traced. For simplification and a basic understanding of receiver operation, the functions are divided into five major divisions (Figure 4-2): Primary Signal (RF, IF and AF), Oscillator Synthesizers, Automatic Gain Control (AGC), Receiver Control, and Power Supply. Additionally, while not a major signal processing section, a functional description of BITE is provided.

The circuit card assemblies associated with the primary signal flow include: A1, A2, A3, A4 and A5. The second major division describes the operation of the oscillator synthesizers (circuit card assemblies A7 and A8) from the first local oscillator signal to the first mixer, the second local oscillator to the second mixer and the beat frequency oscillator function for CW operation. The third division is the operation of the Automatic Gain Control (AGC) which is contained primarily on circuit card assembly A4 along with IF and AF components. Some other AGC circuitry is located on A3 and A5. The fourth division, Receiver Control circuitry which is contained on the front panel and circuit card assembly A6A1, A6A2, and A9, is described. The fifth major functional division of the Receiver is the power supply contained in assembly A10. Figure 4-1 shows an overall functional block diagram of the Receiver and should be followed in reading the description.

4.2.1 Primary Signal – RF/IF/AF Section

The primary signal consists of the Radio Frequency (RF) signal, the Intermediate Frequency (IF) signal, and the Audio Frequency (AF) signal.

4.2.1.1 RF Signal

The antenna signal is connected through the rear panel of the Receiver to a low pass filter located on assembly A1. The four section elliptical low pass filter rejects frequencies above 35 MHz and at the same time prevents local oscillator and IF frequencies from being radiated back through to the antenna. Each section of the filter contains a coil-capacitor tank circuit, with the coil of each stage adjustable for peaking the tank circuit. This provides optimum rejection at its designed frequency. The output of this first low pass filter is routed to another filter located on circuit card assembly A2. This filter operates much in the same manner as the one just described but also provides

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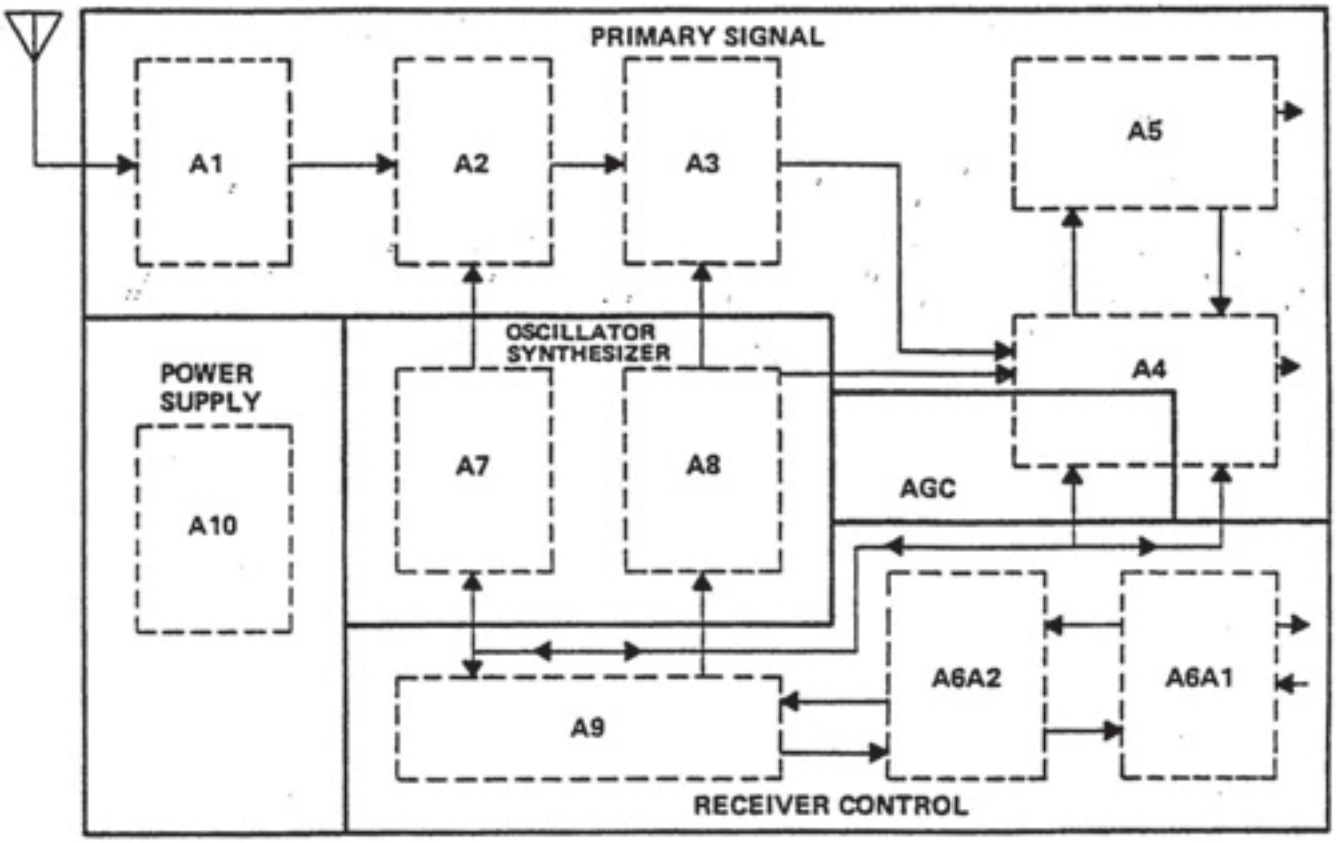

Circuit Card Assembly	Nomenclature	Function
A1	RF Low Pass Filter	Primary Signal
A2	First IF Mixer	Primary Signal
A3	Second IF Mixer	Primary Signal
A4	Main IF/AF	Primary Signal/AGC
A5 (optional)	ISB IF/AF	ISB-Primary Signal
A7	First LO Synthesizer	Oscillator Synthesizer
A8	Second LO/BFO Synthesizer	Oscillator Synthesizer
A6A1 (optional)	Serial Asynchronous Interface	Receiver Control
A6A2	Microcomputer	Receiver Control
A9	Front Panel Control	Receiver Control
A10	Power Supply	Receiver Power

Figure 4-2. Basic Receiver Functional Breakdown

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for impedance matching to the first mixer stage and to reduce peak to peak ripple on the carrier signal. The output of this filter is connected directly to the first mixer where the RF signal is mixed with the variable frequency from the first local oscillator to form the first IF signal.

4.2.1.2 IF Signal

The first IF signal is developed in the first mixer stage where the RF signal is mixed with the variable output frequency of the first local oscillator. The first local oscillator frequency is varied in direct relation to the RF frequency selected from the control section and varies between 40.955 (0.5 MHz selected) and 70.455 MHz (30 MHz selected). This variable frequency produces a different frequency in the mixer of 40.455 MHz. This difference frequency along with all other resultant frequencies is routed to a filter which rejects all other frequencies except the desired 40.455 MHz carrier with intelligence. The filter has a 20 kHz bandwidth and is coupled to a linear buffer amplifier. This amplifier stage is controlled by a control signal from the AGC circuit to maintain a constant amplitude output.

The AGC controlled IF signal is routed to circuit card assembly A3, where it is connected to a two stage IF amplifier, with additional between stage filtering. These two stages provide additional level control of the IF signal. This AGC controlled IF signal is impedance coupled to a band pass filter consisting of four stages of tuned filter traps. An adjustable amplifier just prior to the filters provides for adjusting the gain through the filters. The IF output from the filter is connected to the second mixer where the IF is mixed with the second local oscillator to form the second IF signal. The second local oscillator output of 40 MHz is mixed with the 40.455 MHz first IF, which provides a difference frequency of 455 kHz. This difference frequency is transformer coupled to a filter network which rejects all frequencies except the desired 455 kHz second IF signal. The output of the filter network is coupled to an IF amplifier to restore gain and for coupling to the plug-in band pass filters, contained on circuit card assembly A4.

The IF signal from A3 is coupled directly to seven bandwidth filter slots. The number of filters plugged in and the bandwidth of each filter depends on the option procured. Any number, up to seven, may be plugged into the card at any one time if optional filters were specified. The filter bandwidth desired for operation is then automatically switched into the IF circuit when it is selected from the front panel or remotely. When the optional independent sideband (ISB) is used, filter slot FL1 must contain a lower sideband filter. All bandpass filter slots are permanently connected to a diode switch, including FL1. This filter may be connected, through a movable link, from the diode switch to a bus that leads directly to the ISB circuit card assembly A5.

In all modes of operation, including ISB, the diode switch selects the desired filter slot. The control circuitry automatically selects the filters in an ascending bandwidth order regardless of the order in which they are plugged into the sockets; that is, bandwidth 1 (BW1) selects the narrowest bandwidth and so on with BW5 selecting the widest bandwidth. Two slots are generally reserved for upper sideband (USB) and lower sideband (LSB) which are also automatically selected when that mode is directed from the control section. The IF signal output of the selected bandwidth filter is impedance coupled to a two stage AGC controlled amplifier. The output of this amplifier is then coupled to a bandpass filter for additional filtering of the IF signal. A portion of this signal is routed through a buffer amplifier to J2-IF OUT, on the rear panel, as the IF output signal.

The IF signal is also coupled through a buffer amplifier to one input of an RF switch and to the product and synchronous AM detector. The RF switch also has the beat frequency oscillator (BFO) as an input with the output of the switch coupled directly to the FM detector. The switch has two modes of operation and is switched through the control circuitry. In the AM and FM modes the switch selects the IF signal, in all other modes, the switch automatically couples the BFO to the

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FM detector and limiting amplifier. Two outputs of the FM detector is then coupled to a detector select switch and to the carrier input of the product and synchronous detector. The output to the product and synchronous detector will be either the demodulated AM signal or BFO depending on the mode selected. The detector select switch is also controlled by the function modes of the control section. In the FM mode the select switch passes only the FM detected signal to an audio filter. In all other modes the detector select switch passes the output of the product and synchronous detector to the same audio filter.

When the ISB is selected from the control section, the LSB portion of the IF signal is linked directly to circuit card assembly A5. The flow of the IF signal through the ISB circuit is very similar to that just described; except that the BFO is connected directly to the ISB detector. The USB portion of the IF signal is routed through the A4 circuit card in the ISB mode.

4.2.1.3 AF Signal

The detected audio signal from either the FM detector or the product detector is selected by the detector select switch through receiver control. The selected audio is routed through a lowpass filter to a crosspoint switch. Through receiver control the crosspoint switch selects the various audio modes available as outputs from the Receiver. When the ISB option is installed the audio output from that circuit card is also coupled to the switch. In non ISB modes the main audio (A4 card) is selected and routed to two separate audio amplifiers. The first amplifier is volume controlled through the AF GAIN control on the front panel. The output of this amplifier is routed both to the rear panel for loudspeaker output and to the phones jack on the front panel. The second amplifier is level controlled through a variable attenuator placed in the line to the second amplifier by the crosspoint switch. Attenuation is varied through a screwdriver adjustment on the front panel. This amplifier then drives an output transformer which provides the monitor line output to the rear panel. If the ISB circuit card is installed in this non ISB mode the output of the attenuator will also be routed through circuits on the ISB card and appear on Line 1 output on the rear panel. This circuit is described in the ISB mode which follows.

In the ISB mode either the main (USB) or the ISB (LSB) is selected and routed to the same circuits as described in non ISB mode. In addition the crosspoint switch couples both the LSB and USB through variable attenuators to their respective amplifiers on the ISB circuit card. The two amplifiers drive output transformers which couple the USB (Line 1 output) and LSB (Line 2 output) to the rear panel. Level control of Line 1 output is through front panel screwdriver adjustment MAIN-LINE LEVEL. Line 2 output is controlled through I-LSB LINE LEVEL. These two adjustments vary the attenuators connected in their respective lines.

4.2.2 Oscillator Synthesizers Section

The oscillator synthesizers consist of the first local oscillator (LO) synthesizer, the second LO synthesizer and the beat frequency oscillator (BFO) synthesizer. The three oscillator synthesizers are each independent separate oscillators except that the 1 MHz signal derived from circuitry in the second LO is used as a reference frequency to the other two oscillators.

4.2.2.1 First Local Oscillator Synthesizer

The first local oscillator provides the oscillator frequency to the first mixer where it is mixed with the RF signal to produce the first IF signal. This variable oscillator, located on circuit card assembly A7, is controlled from the receiver control frequency select. It is a voltage controlled single loop synthesizer oscillator with an output frequency variable between 40.955 and 70.455 MHz in 1 Hz increments.

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A voltage controlled oscillator (VCO) generates the basic frequency which is applied to a drive amplifier located on circuit card assembly A2. This same output frequency is applied to the divide-by-N circuit. The value of N is determined by the digital control logic, which is also coupled to the divide-by-N circuit. This digital control logic depends on the RF frequency selection inputs. The output of the divide-by-N circuit is coupled to a phase comparator to which a 100 kHz reference signal and the digital logic is also connected. The basic output of the phase comparator depends on the phase difference between the reference signal and the divide by N signal. This basic output is combined with the digital control logic, filtered and applied to the dc control amplifier. The output of this dc amplifier controls the frequency of the VCO. The output of the VCO is transformer coupled to a high pass filter, located on circuit card assembly A2, which rejects frequencies below the oscillator range. This filter output is applied to a transistor drive amplifier which routes the signal through an RF wideband transformer to the mixer. The VCO is varied between 40.955 MHz (RF selection of 0.5 MHz) and 70.454999 MHz (RF selection of 30 MHz). When this oscillator frequency is applied to the mixer and mixed with the RF signal a difference frequency of 40.455 MHz is obtained. It is this difference frequency that is used for the first IF signal.

4.2.2.2 Second Local Oscillator Synthesizer

The second local oscillator provides the oscillator frequency to the second mixer where it is mixed with the first IF signal to produce the second IF signal. The oscillator, located on circuit card assembly A8, is a constant frequency phase locked oscillator driven from a reference signal. The output of the oscillator is 20 MHz which is frequency doubled to provide the 40 MHz signal to the second mixer. A reference signal, internal or external, is required for operation of the synthesizer. The internal reference signal comes from a crystal oscillator which has an output frequency of 5 MHz. An external reference signal may be applied through the REF IN/OUT connector on the rear panel. The INT/EXT slide switch S2, also located on the rear panel, must be in the appropriate position for the reference selected. With the switch in the EXT position, the internal reference oscillator is turned off and the external reference signal is applied through a transistor switch and shaper circuit to a phase comparator. With the switch in the INT position, access to any external reference is turned off, the internal oscillator is turned on and applied through the transistor switch in the same manner as the external reference.

The heart of the oscillator synthesizer is a 20 MHz crystal reference oscillator whose output is coupled through a buffer amplifier to a divide-by-2, divide-by-2, and divide-by-10 circuit. The resultant 10 MHz, 5 MHz and 1 MHz output of the circuit is coupled to a data select circuit. The 1 MHz signal is also routed to the BFO oscillator and to circuit card assembly A7, where it is used as a reference signal to the first local oscillator. The reference frequency output of the data select circuit is applied to the phase comparator which phase compares this signal to the internal or external reference. The phase difference signal (if any) is then applied through a digital to analog converter to the 20 MHz oscillator. If the oscillator tends to drift off frequency, the phase difference between the reference signal and oscillator signal will be detected by the phase detector and the phase difference, applied through the digital to analog converter, will readjust the oscillator.

The output of the oscillator is also coupled through another buffer amplifier to a frequency doubler. The 40 MHz output signal from this doubler is routed to circuit card assembly A3 and capacitor coupled to the second mixer. The difference frequency between this 40 MHz signal and the 40.455 MHz first IF signal is the second IF signal of 455 kHz.

4.2.2.3 BFO Synthesizer

The BFO provides the fixed and variable beat frequency for reinsertion of the carrier in the sideband and CW modes. The oscillator operates at the second IF signal frequency of 455 kHz and can be varied 8 kHz in either direction. The BFO oscillator, located on circuit card assembly A8, is a

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voltage controlled variable oscillator with a center frequency of 22.75 MHz. The oscillator output frequency is filtered and applied through a buffer amplifier to a divide-by-50 circuit. The output of this divide-by-50 circuit provides the variable 447 to 463 kHz BFO signal for reinsertion at the product detectors on circuit card assemblies A4 and A5.

A digital control circuit is used to vary the basic oscillator frequency of 22.75 MHz. The output of this circuit is coupled to a phase comparator, along with a 500 Hz reference signal. This 500 Hz reference signal is derived by applying the 1 MHz reference signal, from the second local oscillator, to a divide-by-2000 circuit. The phase comparator compares the output of the digital control circuit and the 500 Hz reference signal and applies the difference signal through a digital to analog converter to the VCO. The oscillator may be varied between 22.35 and 23.15 MHz in 500 Hz increments, which when applied to the divide-by-50 circuitry, provides a BFO frequency between 447 and 463 kHz variable in 10 Hz increments. The BFO frequency is filtered before being routed to the product detectors.

4.2.3 Automatic Gain Control (AGC) Section

The AGC circuits provide the Receiver with constant level AF output signal with large variations in the incoming RF signal. For example, the change in IF or AF output levels is less than 6 dB for a change in the input level of −100 dBm to −10 dBm. This automatic gain control is accomplished through AGC circuitry, located mainly on circuit card assembly A4. The optional ISB circuit card assembly A5 contains its own AGC for signal gain control in the ISB mode of operation.

The Receiver may be operated in any one of three different gain control modes: manual, automatic, and automatic with a manually set threshold. In the manual mode, the gain is set through a front panel control. In the automatic mode, the AGC circuits will compensate for changes in the receiver input signal level. In the automatic/manual mode, the front panel control is used to set the operating threshold of the AGC circuits.

The AGC operates from a portion of the IF signal taken after the gain control IF amplifier stage, thus maintaining a closed AGC loop. The AGC detects the IF signal, provides three different decay times, and provides for automatic threshold control of the output signal or manual threshold control. The output of the AGC circuit is routed to the second IF amplifier on circuit card assembly A4 to a current amplifier on circuit card assembly A3. The current amplifier controls the first IF signal by controlling the gain of two IF amplifier stages; one located on circuit card assembly A3 and the other located on circuit card assembly A2.

4.2.4 Receiver Control Section

Signals that control the receiver's operational parameters (such as operational mode, receiver frequency, BFO frequency, bandwidth, AGC and BITE sequence) are produced by the microcomputer (A6A2) and routed by the front panel receiver control circuit card assembly (A9). The microcomputer under program control follows instructions it receives from the front panel in LOCAL operation and from the remote controller in REMOTE operation. In both LOCAL and REMOTE, the microprocessor functions essentially the same; however, when being operated from a remote location, the power must be turned on at the front panel and the optional serial asynchronous interface assembly (A6A1) must be installed. The serial asynchronous interface circuit card assembly (A6A1) interfaces the external remote controller (when used) with the microcomputer.

Figure 4-1 shows the receiver control circuits and shows the signal flow between the front panel receiver control assembly (A9), the microcomputer circuit card assembly (A6A2) and the serial asynchronous interface circuit card assembly (A6A1). The front panel receiver control assembly (A9) contains the Liquid Crystal Displays (LCD), connects to both sets of keyboard switches

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and the receiver control circuits and routes data between these units and the microcomputer. The RA6790/GM interconnections diagram contained in Section VII show all connections to and from these modules.

As shown in Figure 4-1, the microcomputer (A6A2) directs receiver operations by interfacing with circuits on the receiver control assembly (A9) and serial asynchronous interface (A6A1) and sending control signals to various receiver circuits. The receiver control assembly (A9) contains the tuning mode and frequency displays and the tuning control circuits and connects to the frequency select and the modes select keypads. The strobes and selection circuits that route data under microprocessor control are also on the receiver control assembly. The strobe and selection circuits control the transfer of information between the front panel and the microcomputer as well as between the microcomputer and the receiver circuitry.

The basic functions performed by the microcomputer (A6A2) include:

1. Initialize circuits following power application.
2. Read local input signals from front panel controls.
3. Update front panel displays.
4. Compute and send receiver tuning and operating data to the appropriate receiver circuits.
5. Receive commands from the remote controller and upon request, return receiver status.
6. Retain memory of receiver setting at power failure or turn-off and restore receiver to the operational modes when power is reapplied.

The microcomputer directs receiver operations by executing the control program that it obtains from the Erasable Program Read Only Memory (EPROM). During local operation, the receiver is controlled by the microcomputer as follows:

a. The frequency and mode setting established by the front panel switches and the tuning control are continuously read at 25 ms intervals by the microcomputer. The actual scanning function of the microcomputer is under program control. As the microcomputer scans the front panel switch and controls, it also stores the current status of each control parameter in the memory (RAM).

b. The microcomputer, again under program control, uses the stored control parameters that it placed in memory to compute the control signals that it sends to the receiver circuits (1st LO Synthesizer, 2nd LO and BFO, and main IF/AF). These digital control signals are then sent to the receiver circuits through the receiver control assembly (A9) to generate the desired operation.

c. Periodically, as established by the control program, the microcomputer reads the receiver status that it has stored in memory (RAM) and sends this information to control the front panel displays.

d. When the microcomputer senses a BITE (Built In Test Equipment) request from the front panel switches, it is directed to perform the BITE test sequence and follows the BITE program which is also contained in memory. During BITE sequence the processor disables all external and local controls.

NOTE

The receiver control program and the BITE program have been developed by the manufacturer as part of the receiver design and cannot be changed or updated by the customer for either operational control or maintenance.

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During remote operation, the receiver is controlled by the microcomputer, but in place of instructions from the front panel, the instructions to the microprocessor are obtained from the remote controller:

1. During the front panel scan, the microprocessor monitors the position of the LOCAL-REMOTE switch. When this switch is in REMOTE, the microprocessor will branch to the remote mode portion of the program so that instead of responding to front panel switches, it will look for command words from the remote interface card (A6A1).

2. Commands from the remote controller are received by the Serial Asynchronous Interface Assembly A6A1. As each command is received, an interrupt is sent to the microcomputer which directs the microcomputer to branch to specific portions of the program (or subroutine) to carry out the command. After responding to the command instructions, the microcomputer returns to the normal remote mode program until a new set of commands or requests are received from the remote controller.

3. When the remote controller contains data for receiver control (such as frequency, AGC, or mode selection) the microcomputer stores the data in memory (RAM), and on completion of remote data interrogation transfers the information to the receiver circuits.

4. When the remote controller command contains a request for receiver status, the microprocessor accesses the corresponding receiver status information stored in memory (RAM) and sends it via the Serial Synchronous Interface Assembly (A6A1) to the Remote Controller.

5. In addition, the microcomputer under program control periodically (every 25 ms) reads the receiver parameters from memory (RAM) and continually updates the front panel displays.

When a request is received from the remote controller during LOCAL operation, the microprocessor will respond and return the status of the receiver as described in the above paragraphs. Remote commands received during LOCAL operation will be stored in memory but they will not be acted upon unless the receiver is placed in REMOTE operation.

The microcomputer directs all operations and communicates with other receiver control circuits through its 8 bit bi-directional data bus and the write/read and clock (ROMC) lines. The ROMC lines indicate the type of instructions to be performed with the write and clock lines providing the necessary information. The 8-bit bus provides both bi-directional data and unidirectional address capability (to the Receiver). The operating control program is contained in the program memory EPROMS (Erasable Program Read Only Memory). Temporary storage for receiver settings and for data computations is provided by the Working Random Access Memory (RAMs), which can be written into and read out of by the CPU. These memories are addressed by the CPU, through the static memory interface (SMI). The CPU sends the ROMC, write and clock signals to the SMI. The SMI recognizes the ROMC code calling for a Memory Address operation. The SMI, in sequence, addresses the ROM or RAM over the memory address bus. Then it sends a read signal to the EPROM (if it is addressed) or sends a read or write signal to the RAM (if it is addressed). The CPU places the data to be read by the RAM on the data bus or reads the data placed on the data bus by the ROM or RAM, as appropriate.

The microcomputer (A6A2) also contains the RESET and RAM data retention circuitry. The RESET circuitry generates reset signals when power is applied and turned off. This reset signal is applied to the CPU. When power comes on, the CPU initializes all circuitry to its starting condition and causes the program to start at its initial program address. When power is removed, due to power turn-off or power failure, the reset signal to the CPU goes low. The CPU now causes the system to

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come to an orderly halt. In addition, the memory data retention circuitry (at power turn-off) connects an internal battery to the RAMs so that the receiver settings are retained in this memory. Thus when power is reapplied, the receiver will be reset to its last operational condition when power was interrupted. Also, at power turn off, the memory retention circuitry places the RAM in a lower power drain mode which retains memory but draws a minimal amount of power from the internal battery. When external power is applied, the internal battery is charged by the external power supply.

The CPU, in programmed sequence, receives and sends data from and to the front panel displays and controls, and the receiver control circuitry (through A9) via the CPU data bus. The data is directed between the CPU data bus and the receiver control and front panel circuitry, in the correct program sequence, by the bi-directional, tri-state switch. This switch is controlled by the strobe logic which is driven by the ROMC, write and clock signals from the CPU. The addressing of the various receiver and front panel circuitry, to accept or supply data from or to the data bus, in the prescribed program sequence, is done by the strobe logic and tri-state latched switch. This switch is driven by the CPU data bus and its outputs latched to the input data from the bus, at the prescribed program times, by the strobe logic.

The CPU receives and sends data from and to the remote controller via the Serial Asynchronous Interface (module A6A1). Data to and from the CPU and module A6A1 is sent directly over the CPU data bus. Additional control signals between the CPU and the module A6A1 are sent via the CPU I/O (input-output) ports. A UART (Universal Asynchronous Receiver Transmitter) in the A6A1 module interfaces the parallel 8-bit data word on the CPU bus to the serial data streams in and out from and to the remote controller. The UART also generates and sends to the CPU an interrupt request whenever the remote controller sends commands or data. This requests the microcomputer to orderly stop its present program and jump to a program routine which will service the remote controller commands and data. The UART and interrupt logic on the A6A1 module will supply the CPU with the interrupt routine starting address by placing this interrupt vector address on the CPU data bus when the CPU acknowledges that it will service the interrupt request. The reset signal from the microcomputer module is also sent to the interface module to initialize its circuitry at power turn-on.

As indicated in the block diagram, Figure 4-1, the front panel receiver control, module A9, connects to the keyboard switch panels 1 and 2. These switches are continually read. in program sequence, by the CPU. The switches are read in groups, with the switches being selected by enabling their associated data select buffers. The data select and strobes circuitry selects the buffers, in the programmed sequence, as directed by the strobe logic and tri-state latched switch outputs from the microcomputer A6A2. The read data goes on to the buffered data bus and then through the data buffers and the bi-directional, tri-state switch to the CPU bus. It should be noted that the digital outputs from the tuning knob encoder and digital data outputs from the IF/AF (A4 module) are read out here as if they were additional switches.

Both the tuning mode and frequency indicating front panel Liquid Crystal Displays (LCD) are contained on module A9. These displays are continually updated by the microcomputer CPU.. The displays are driven by decoder-drivers which are enabled by their respective data select and strobes. The data from the CPU bus is applied to this circuitry, at the correct times in the program sequence, through the data buffers and bi-directional tri-state switch. The operating and tuning data developed by the microprocessor is relayed to the appropriate receiver circuitry through module A9. The buffered data bus goes directly to the main IF/AF module, A4, with the data select and strobes circuitry supplying the strobes to the various circuits in this module. Data to the 1st LO and 2nd LO/BFO modules are generated, in the proper program sequence, through the data select and strobes circuitry in the A9 module. Data to the 1st LO consist of a strobed and clocked serial data stream. The 2nd LO/BFO data consist of a binary coded digital word for the BFO frequency and an ON-OFF signal for the BFO. It should be noted that OOL (Out of Lock) signals from the 1st LO, REF and BFO drive

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the OOL indicators located on the A9 card. The OOL overall signal, generated by the microcomputer, is sent to the front panel OOL indicator through A9.

The serial asynchronous interface module, A6A1, in addition to the UART and interrupt circuitry described earlier, contains circuitry for selecting and generating serial data mode and baud rates and for setting the receiver address when the receiver is used in the remote mode.

4.2.5 Power Supply Section

The power supply provides the various dc voltages required throughout the receiver. The unit, located on assembly A10, contains a step-down transformer, diode rectifiers, filter capacitors and regulators. Primary input power is controlled through a POWER ON switch located on the front panel. This primary input power may be either 100, 120, 220 or 240 volts from 43 to 420 Hz. The proper voltage is selected through a pc wafer and voltage selector located on the rear panel of the receiver. The step-down transformer provides three different voltages for rectification, filtering and regulation. Six different dc voltages are provided at the output of the power supply. These voltages are +20 Vdc regulated, +15 Vdc regulated, +15 Vdc unregulated, −15 Vdc regulated, +5 Vdc regulated and +5 Vdc unregulated.

4.2.6 Built In Test Equipment (BITE) Functional Description

The BITE system of the receiver has the ability to perform two major functions. First, it determines, organizes and displays the bandwidth of the IF filters installed in the receiver. This allows the installation of these filters in any slot, with minimum limitations. Secondly, the BITE performs tests of functionality of the receiver modules. These tests provide overall verification of the operation of the receiver, and specific verification of the operation of selected modules. The BITE performs the following functional tests in the receiver: Readability of the RAM in the microcomputer; lock condition and timing of all phase locked loops; settling time in the frequency synthesizers; operation of the IF AGC; operation of the ISB AGC detector if it is installed; and measuring the bandwidth of all of the IF filters. In order for the receiver to pass the above tests, all modules must have been operating properly. However, A1, A6A1, A4 and A5 are not interrrogated.

BITE may be controlled by the operator from the front panel of the receiver through the simultaneous use of two controls, one on each keypad. This minimizes the likelihood of accidental interruption of an operating receiver. To initiate BITE from the front panel, the operator must press both the LOCK and the AM pushbutton switches, then release AM and then LOCK for initialization. The microcomputer then begins the full BITE sequence. As the microcomputer is executing the BITE program, the front panel display indicates what the receiver is actually doing. For instance, frequency, BFO and mode data are displayed. Should an error be discovered the front panel frequency display is blanked except for a two digit error code which contains the number of the test that failed. The operator writes down the number of the test that failed then pushes both LOCK and CW and then releases CW and then LOCK, which tells the microcomputer to continue to the next test. The displays are reinstated and the testing proceeds. The displays remain active throughout the tests since the process takes approximately one minute to complete, and if the displays are moving, the operator has confidence that the tests are proceeding. When the test is finished, the receiver will return to the signal it was monitoring prior to being told to perform the BITE test sequence. Should the operator wish to terminate the BITE cycle at any time, he may press and hold LOCK and LSB then release LSB then LOCK and the receiver will revert to its normal pretest operation at a point in the sequence where disabling the process is allowed. In addition to being able to originate the test, to continue the test, and to stop the test, there is (for maintenance purposes) a loop facility which can be invoked by using both LOCK and USB pushbuttons. In this mode, the front panel controls, with the exception of LOCK and USB, are disabled but the microcomputer will continuously supply the signals required to perform the failed test so that additional fault isolation procedures, using external test equipment, may be employed.

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The BITE sequence may also be initiated by a remote device. The remote control device sends a message to the receiver telling it to initiate BITE. BITE will then report up to a maximum of five errors and then report a test complete code upon request. If the test complete code is received with no fault numbers, then the receiver passed the BITE tests. The control device may send a message to the receiver asking for the installed IF filter bandwidths. The receiver would then send the measured bandwidths to the controller showing the filter slot positions in which each filter is installed.

During initialization, BITE is initiated if the microcomputer determines that the memory has been corrupted for some reason. This automatically initiated BITE will determine the receiver filter complement, organize a filter assignment table, and return the receiver to operation. When performing this test, the receiver does not stop on errors but completes the testing and restores receiver operation. The receiver also does not stop on errors when BITE is initiated under remote control, but completes the sequence and stores the fault numbers for remote interrogation. The following discussion describes the actual tests conducted to verify the proper operation of each module.

a. Microcomputer. All 256 bytes of the Random Access Memory (RAM) in the microcomputer are tested to ensure that the memory may be written into and read out of properly. A ones and zeroes memory pattern is used to perform this test.

b. Second Local Oscillator and BFO. The lock status of both the BFO and the second local oscillator synthesizers is tested. The second local oscillator synthesizer should be locked at all times. The BFO is enabled by placing the receiver in the CW mode. The BFO synthesizer is then tested for a lock condition both at 455 kHz and all 500 Hz steps between and including plus and minus 8 kHz offsets. This dynamic program also checks the switching times of the BFO synthesizer as indicated by the out-of-lock circuitry on the BFO board. A failure in any of these tests is indicated as an error code to the operator or to the remote controller, on request.

c. First Local Oscillator. Testing of lock, in 500 kHz intervals from 30 MHz to 0 MHz, is performed, and the switching time of the synthesizer throughout the band is tested utilizing out-of-lock signals as the indication for reaching lock after each step.

d. IF Module. The IF module (A4) is checked to determine whether or not the AGC circuits operate properly on signals. The test routine enables the CW detector and BFO, and checks that an audio output is present during the initial filter tests. The manual IF gain attenuation system is tested by observing its control effects on the audio output level during the filter tests.

e. ISB Module. When the optional ISB board (A5) is installed it is checked for proper AGC action along with the IF gain and the manual IF gain control, in the same way that the main IF board (A4) was checked.

f. IF Filters. One of the major functions of the BITE is to determine the bandwidths of the IF bandwidth filters installed in the receiver, and assign them to bandwidth selection switches BW1 through BW5. The filters are assigned in order of increasing bandwidth and allow the operator to select a desired bandwidth. In addition, two different types of single-sideband detection filters may be used and the bandwidth determination routines verify their correct installation. Two sideband filters may be installed in the receiver for independent or normal sideband operation. one for upper sideband, the other for lower. (When ISB is installed these two filters are required.) If one symmetrical sideband filter is to be used for both sidebands it may be installed in filter slot FL1. Then for lower or upper sideband, the first and second local oscillators are offset by 1.8 kHz to accommodate the symmetrical filter. There is one restriction on the filter complement in the receiver; the FL1 slot must contain the filter to be used for lower sideband. It may be either the independent offset sideband filter or a symmetrical filter, but in either case it must be the filter used for lower

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sideband. The BITE bandwidth routine checks the filter in the FL1 slot to determine whether or not it is a center-tuned filter or an offset filter. If center tuned, it uses the filter for both sidebands by putting a 1.8 kHz offset in the first and second local oscillator. If it is an offset filter, the filter slot that the filter is in is labeled for the lower sideband and the rest of the filter complement is searched for the matching USB filter. If a symmetrical filter is found to be installed in the FL1 slot, the offset for the first and second local oscillators is set to 1.8 kHz; however, if an offset sideband filter is found with a symmetrical filter in FL1 slot an error will occur. If there are less than 5 symmetrical filters installed in the remaining slots of the receiver, the symmetrical filter in FL1 is used as a center tuned filter which may be used for the AM, FM, or CW detection mode. If five other filters are present in the system, the symmetrical sideband filter will be used only for sideband reception. The remaining filter slots, FL2 through FL7, are checked for presence of a filter, except for a slot which has previously been identified as the USB slot. If there is a filter present in a slot, its bandwidth is measured. The first LO is scanned, in frequency, from a 10 kHz maximum offset back to the 3 dB point, based on a previously measured center frequency reference level. (NOTE: This reference level can vary from filter to filter.) The frequency difference between the center referenced level and the 3 dB point is designated as half the actual bandwidth. Having measured the bandwidth of all the filters installed. the filters are sorted in order of increasing bandwidth so that when the BW1 pushbutton switch on the front panel of the receiver is pressed, the narrowest bandwidth available is selected. When the BW2 pushbutton switch is pressed, the next narrowest progressing to the widest at BW5 (if there are less than 5 symmetrical filters installed in slots FL1-FL7 the widest one is assigned a number corresponding to the maximum number of symmetrical filters installed). Future filters which may have different bandwidths from the filters presently defined may be used in this system without any change. The bandwidths of the filters installed in the receiver can be reported to the remote controller upon command. In the remote operating mode, if the remote controller asks for a specific bandwidth, the receiver selects the bandwidth that is nearest to the bandwidth requested. The Receiver reports the actual bandwidth used to the remote controller. This is an indirect check on the filters.

4.3 DETAILED CIRCUIT DESCRIPTION

This section provides a detailed description of all electronic circuits contained in the receiver. Refer to Figure 4-1 for an overall functional block diagram. Figure 4-2 lists the circuit card assemblies in the order that they are described in the following paragraphs. Simplified functional block diagrams along with timing diagrams and tables are used throughout the text to aid in simplifying the description. Components referred to throughout the text are referenced by their last two reference designators. Block diagrams referred to throughout the text should be used in conjunction with applicable schematic diagrams in Section VII.

4.3.1 RF Low Pass Filter, A1

The incoming RF signal is passed from the RF IN connector J1 to a 50 ohm, 4 section elliptical lowpass filter which has a cut-off frequency of 35 MHz (refer to schematic diagram, Figure 7-1). This filter provides the necessary protection to the Receiver from image signals at frequencies between 81.4 and 111.4 MHz; and from signals at the first intermediate frequency of 40.455 MHz. The filter also prevents first local oscillator reradiation from the antenna connection. Each section of filter consists of a tank circuit, consisting of a tunable coil (L1 through L4) and capacitor (C2, C4, C6 and C8). connected sequentially in the receiver line with a second capacitor (C1, C3, C5, C7 and C9) connected from each tank circuit parallel to the signal flow. Each tank circuit is tuned to provide a high resistance to a particular frequency while other frequencies are reflected in the parallel capacitor which in turn reflects this signal to the next stage and so on.

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4.3.2 First Mixer, A2

Figure 4-3 is a simplified block diagram of the first mixer module A2. It consists of a signal lowpass filter, first mixer, bandpass filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the first local oscillator frequency of 40.955 to 70.455 MHz. The schematic diagram for the first mixer is shown in Figure 7-2.

4.3.2.1 RF Signal Lowpass Filter and Mixer

The output of the A1 module is connected to the first mixer through a two section elliptical lowpass filter (L15-C23, L11-C24-C25 and L12-C26-C27), which has a cut off frequency of 35 MHz and serves to present a defined impedance to the mixer, U1, RF input port. This filter operates much in the same manner as the RF input filter, except the first input coil L15 is non-adjustable. It offers a very low impedance to the incoming wanted RF signal, but an increasingly higher impedance to frequencies above 30 MHz. The mixer U1, is used for mixing both the incoming RF signal (0.5 to 30 MHz) and the first local oscillator signal (40.955 to 70.455 MHz). The resultant frequencies are taken from the mixer, and filtered to provide a difference frequency of 40.455 MHz to form the first IF signal.

4.3.2.2 First Local Oscillator Input Filter and Drive Amplifier

The filter for the incoming first local oscillator signal is comprised of four sections of a tunable coil (L1 to L4), connected in series with a capacitor (C2, C4, C6 and C8) and with the combination of the two connected parallel to signal flow. A second capacitor (C1, C3, C5 and C7), connected in series with signal flow separates each coil capacitor. Each coil is tuned for maximum impedance for a desired frequency. The series capacitance acts as a high impedance to undesired frequenices below 40 MHz. The output of this filter is coupled to a common emitter amplifier Q2 through capacitor C9 and resistor R3. The mixer drive amplifier is comprised of transistors Q1, Q2, Q3 and Q4. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of common emitter amplifier, Q2, whose current is regulated by transistor Q1. The voltage at the base of Q1 is set by divider R1 and R2 which in turn sets the potential at the emitter of Q1. Thus the current through R6 is regulated by bias control of Q2 via R6 and L6. The output of Q2 is capacitance-coupled (C21 and C22) to a complementary pair amplifier made up of PNP transistor Q3 and NPN transistor Q4. The output of this pair is applied directly to transformer T1 to drive the LO input to mixer U1. The mixer also receives the RF input from A1 as described above.

4.3.2.3 AGC Controlled IF Amplifier

The output of the mixer is coupled to a bandpass filter FL1. This crystal bandpass filter is designed to reject all the resultant mixer frequencies, except the difference frequency of 40.455 MHz with a bandwidth of 16 kHz. This 16 kHz bandwidth provides an additional option in the AM, FM, or CW modes of operation. This first IF signal is coupled through C44 to an impedance matching network of L16, C32 and R14, and to a linear amplifier consisting of field effect transistor Q5. A dual tapped transformer T3, makes up part of the load circuit of Q5, to which is connected a current controlled AGC signal. This AGC signal, in effect, varies the impedance of the load transformer which in turn varies the gain of Q5. A second signal from the AGC circuit is applied to the gate of Q5 which varies its bias in relation to the AGC signal strength. This results in a high linear AGC controlled first IF signal, for output to the second mixer circuit card assembly A3.

4.3.3 Second Mixer, A3

Figure 4-4 shows a simplified functional block diagram of the second mixer circuit card assembly A3. It consists of a three stage AGC controlled first IF amplifier, a bandpass filter, a mixer

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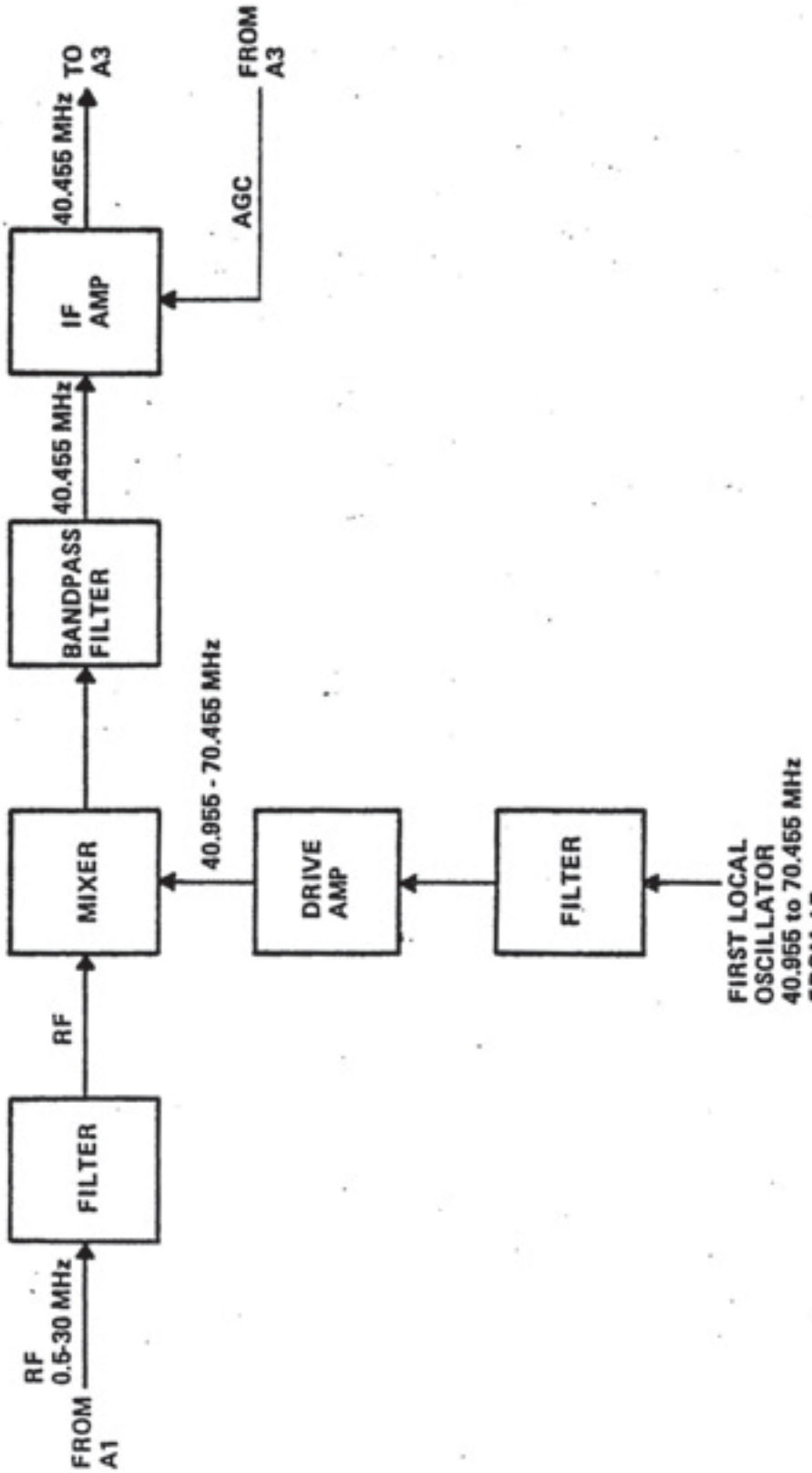

Figure 4-3. First Mixer, Functional Block Diagram

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and output second IF amplifier. Input signals to the circuit card include; the first IF signal from A2, AGC signal from A4, and the second local oscillator signal from A8. The output signals consist of AGC output to A2 and the second IF signal to A4. Figure 7-3 shows the schematic diagram for the second mixer, A3.

4.3.3.1 First IF Amplifier

The first IF amplifier consists of three stages with the second stage gain controlled from the AGC signal. The third stage drives the signal for input to the bandpass filter. The 40.455 MHz signal routed from A2 is coupled to the drain of field effect transistor Q1, through capacitor C1. The grounded gate of this stage provides high gain for input to filter FL1 through capacitor C5. Filter FL1 provides for rejection of all frequencies other than the 40.455 IF signal. The output of the filter is connected through capacitor C6 to the drain of field effect transistor Q2, which also has a grounded gate. The load circuit of Q2 consists of resistors R16 and R18 and a dual tapped transformer T1. The AGC signal is connected to one tap of the transformer and, in effect, varies the impedance of the load transformer. This action varies the gain of the amplifier in relation to the AGC signal. The output of this stage is taken from the second tap on the transformer and coupled to the base of NPN transistor Q3, through capacitor C11 and resistor R20. A variable coil that forms part of the first section of a four section bandpass filter is connected into the load circuit of Q3. The output of Q3 is, therefore, reflected directly into the bandpass filter. A variable resistor R26 in the emitter circuit of Q3 provides for gain adjustment of this stage.

4.3.3.2 Bandpass Filter, Mixer and Second IF Amplifier

The bandpass filter consists of four tunable tank circuits (C15-L5, C16-L6, C17-L7, and C14-C19-L8), each made up of a tunable coil and a capacitor. Each stage is tuned to resonate at the first IF signal frequency and reflects its output to the next section for finer tuning and so on. The output of this filter is coupled directly to the input of integrated circuit mixer U3. A 40 MHz signal from the second local oscillator is connected to a second input of the same mixer. It is this difference frequency that is used as the carrier for the second IF signal. All other frequencies are rejected through the filter consisting of capacitors C31 and C32 and coil L9. The output of the mixer, U3, is connected to a tapped load transformer T2. The output is taken from that transformer tap and coupled through C24 and the filter, just described, to an integrated amplifier U4. This stage provides amplification for the second IF signal output from A3.

4.3.3.3 AGC Amplifier

A two section AGC amplifier is contained on circuit card assembly A3 which provides for both voltage and current control of a signal from AGC circuits on A4. This controlled AGC signal is applied to two IF signal stages for level control. One of the IF stages controlled is located on circuit card assembly A2 and described in paragraph 4.3.2.3. The second AGC controlled IF amplifier is on A3 and is described in Paragraph 4.3.3.1. An AGC signal from the AGC circuit on A4 is routed through resistor R2 to two separate amplifiers. The first amplifier is a two stage feedback amplifier consisting of integrated operational amplifiers U2B and U2C. The highly regulated output of this amplifier is routed to circuit card assembly A2 and used as the bias control to the gate of that output IF amplifier. The same AGC signal through resistor R2 is routed to an integrated operational amplifier U2A. This amplifier has both its negative and positive inputs regulated through voltage regulating transistors U1A (positive) and U1B (negative). The action of these transistors control the bias voltage to the operational amplifier which in turn controls its output current flow. The output of this amplifier stage is then coupled to transistor U1C which amplifies the signal and applies it to the IF amplifier through resistor R19 and diode CR1. The diode prevents IF signal feedback to the amplifier. This signal then controls the gain of that IF amplifier in relation to the AGC signal from A4. The output of the operational amplifier U2A is also coupled to the base of transistor U1D which buffers the signal for application to the IF amplifier stage on A2.

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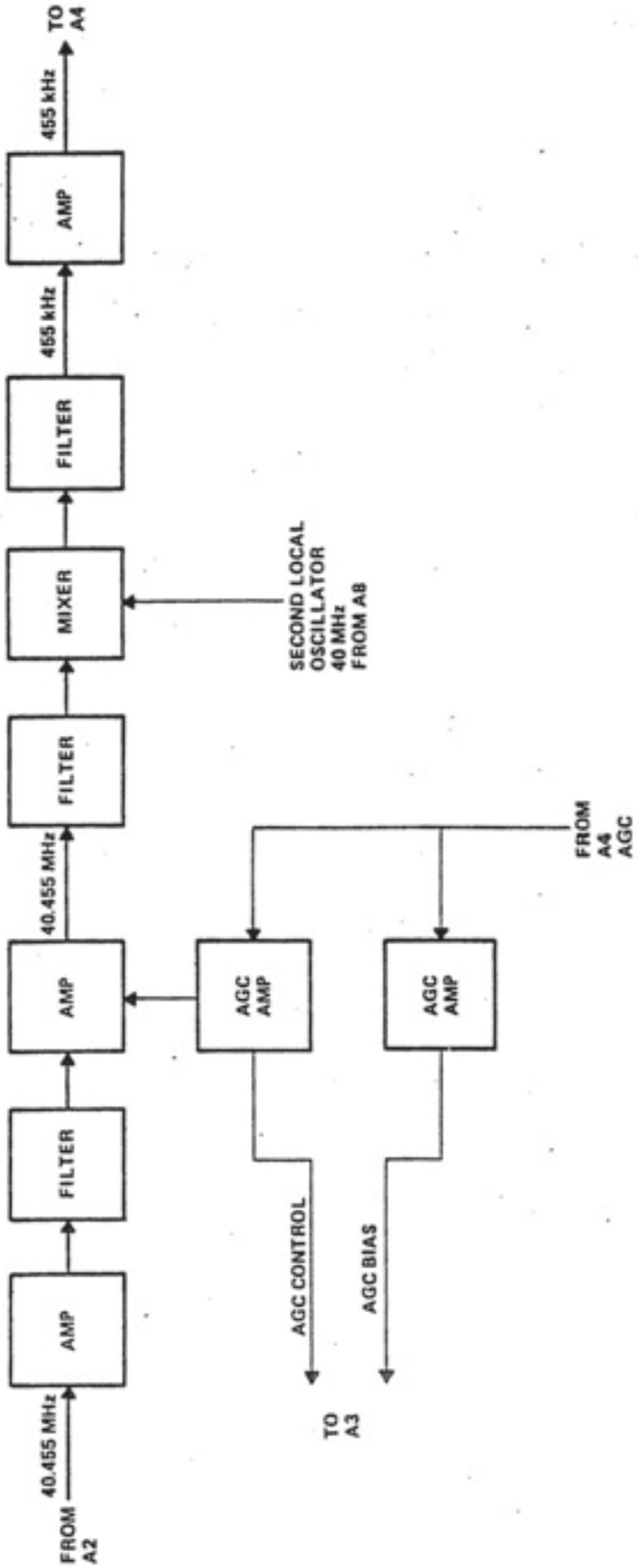

Figure 4-4. Second Mixer, Functional Block Diagram

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4.3.4 Main IF/AF, A4

The Main IF/AF circuit card assembly A4 contains IF circuits, AF circuits, and AGC circuits. The description of these circuits are divided into those three basic functions and shown in three separate simplified block diagrams in Figures 4-5, 4-6, and 4-7. Receiver control circuits are also contained on A4 and are described under the A9 circuit card. Input signals to the circuit card include: the second IF signal from A3, the BFO signal from A8, audio and AGC signals from A5 and control signals from A9. Output signals from the board include: second IF signal to A5, BFO, audio and AGC signals to A5, audio signals to A9 and to the rear panel, AGC signals to A3, and control signals to A9. The schematic diagram for the A4 circuit card is shown in Figure 7-4.

4.3.4.1 IF Circuits

Figure 4-5 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4. This circuitry consists of the bandpass filters, their switching circuitry. a four stage IF amplifier, an IF output amplifier, an RF switch, a limiting amplifier and FM detector, and a product and synchronous AM detector. The second IF signal routed from A3 is connected directly to seven 455 kHz bandpass filter sockets FL1-FL7. These sockets provide for plugging in up to seven optional preselected filters of various bandwidths. These filters optionally available in bandwidths from 0.4 kHz to 16 kHz, may be changed at the customer's discretion, (refer to Section 1). Selection of a particular installed filter is then accomplished automatically through the receiver control system. Each filter socket is connected to a diode switch which is controlled from the receiver control circuits. The output of the diode switch for filter FL1 must be linked to the common output of all the other filter switches, if it is used in A4 operation. If it is to be used for the ISB operation, then it must be linked to the output for that circuit card assembly A5. The receiver control is programmed to select and switch into the circuit the filters in ascending order of bandwidths, regardless of the order in which they are plugged into the sockets; that is, when BW1 is selected, from receiver control, the narrowest bandwidth contained in the seven sockets (six if ISB is installed) will automatically be selected. BW2 will select the next widest bandwidth and so on with BW5 selecting the widest bandwidth. Two filters are generally reserved for USB and LSB operation, which are also selected automatically when those modes of operation are called for through receiver control.

The common output of the diode switch which consists of CR1 through CR14, R9 through R22 and C21 through C27, is connected through resistor R25 to the base of transistor Q1. This emitter follower stage acts as a buffer between the diode switch and the input to a two stage IF amplifier U8 with AGC control. An incoming AGC signal is applied to each stage of the integrated circuit amplifier and provides for level control of the IF signal. A variable resistor R39 connected between the output of the first stage and the input of the second stage provides for manual adjustment of the gain of the IF signal. Variable resistor R47 is used for adjusting the AGC signal level. The output of the two stage IF amplifier is connected to a filter consisting of capacitors C44, C46 and C47, resistor R50 and tunable coils L1 and L2. This double tank circuit provides for rejecting unwanted spurious signals. The output of the filter is routed through capacitor C49 to two separate functions; a three stage IF output amplifier and an emitter follower amplifier Q6. The first stage, Q7, of the IF amplifier is an emitter follower which provides buffering between the incoming signal and the second stage Q8. This second stage amplifies the signal and connects it to still another emitter follower stage Q9 for buffering to the IF OUT connector J2, located on the rear panel.

The emitter follower amplifier Q6 acts as a buffer in the same manner as Q7 above but its output is routed to three separate functions; the AGC detector circuit, the product detector and the FM detector through the RF switch. The signal routed to the AGC detector is described under AGC control circuits. The IF signal routed to the FM detector U18 through the RF switch

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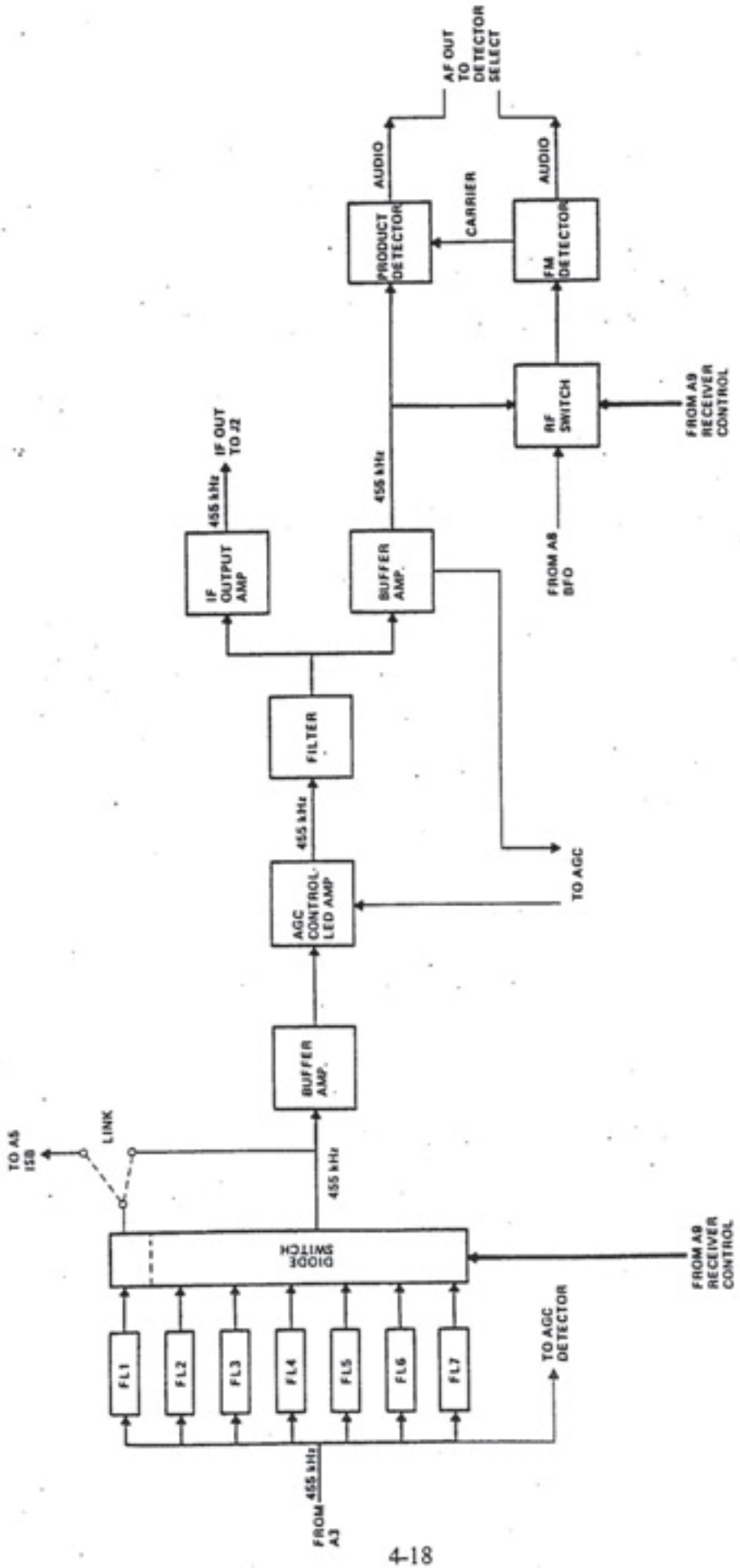

Figure 4-5. A4 IF Circuits, Functional Block Diagram

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CR22-CR25 is (a diode switch) operated by Receiver control. Receiver control directs the switch to connect the IF signal to the detector in the AM and FM modes only. In all other modes of operation, the RF switch connects the BFO signal to the FM detector U18. The IF signal routed to the product detector is connected to its signal port. All signals applied to the FM detector; AM, FM or BFO are connected to a limiting amplifier which removes modulation from the AM carrier and passes it or BFO through the output carrier of the FM detector to the carrier input of the product detector. In the FM mode the signal is detected, its carrier rejected, and an audio signal, from the detector audio output, is connected to the detector select switch. This switch, an integrated circuit transistor gate U19A will select the detected FM audio, only in the FM mode, as directed by receiver control. In all modes except FM, a carrier frequency (AM or BFO) is applied to the carrier input of the product detector. In all modes of operation the signal selected, through receiver control, appears on the signal input of the detector. The detector removes the carrier and routes the audio, through its output, to the detector select switch U19A described above. Receiver control directs this switch to select that audio in all modes except FM.

4.3.4.2 AF Circuits

Figure 4-6 shows a functional block diagram of the audio circuits contained on circuit card assembly A4. This circuit consists of an audio lowpass filter stage, a crosspoint switch, two attenuators and two output amplifiers. The audio signal from detector select U19A is connected, through capacitor C85, to a lowpass filter and amplifier U28. The filter rejects any unwanted frequencies above the audio frequency that might have passed through the detector. The amplifier U28 operates in two different modes. In the AM and FM modes transistor switch U19B disconnects capacitor C113 from the circuit while in all other modes the capacitor is connected across R128 effectively shunting this resistor; thus reducing the signal level in these modes. The output of amplifier U28 is connected to an audio crosspoint switch U25. This switch, through Receiver control, controls audio switching from A4 circuits described above and from the optional A5 circuit card when installed. In non ISB modes the switch routes the A4 signal to the AF GAIN input and to variable attenuator U30. The signal through the AF GAIN control is coupled through capacitor C96 to an audio output amplifier U26. The output of this amplifier is coupled through C108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal through the AF GAIN control is coupled through capacitor C 108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal through variable attenuator U30 is routed to connector J8 for output to the ISB circuit card and is also routed back to the crosspoint switch. The switch, in this non ISB mode, connects the attenuated signal through capacitor C95 to a second audio output amplifier on integrated circuit U26. This amplifier drives transformer T1 through C107 and is coupled to the Monitor Line output on connector J3 on the rear panel. The variable attenuator is controlled through screwdriver adjust MAIN-LINE LEVEL located on the front panel and provides level control of the main (A4) audio signal to the Monitor Line output in the non ISB mode.

In the ISB mode either main (USB) or ISB (LSB) is selected and routed to the same circuits described in non ISB mode. In addition the crosspoint switch couples both the USB and LSB through variable attenuators to their respective amplifiers on the ISB circuit card. The USB is routed through attenuator U30 and controls the signal as described in non ISB mode. The LSB signal is routed through attenuator U31 to J8 and back to the crosspoint switch in the same manner as USB. Attenuator U31 is controlled through screwdriver adjust I-LSB LINE LEVEL located on the front panel and provides level control of the LSB (A5) audio signal. The LSB and USB are routed through connector J8 to their respective amplifiers on circuit card A5 and returns through circuit card A4 to Line 1 Output (USB) and Line 2 output (LSB) on AF OUT Connector J3 on the rear panel.

Two audio signals are routed to the AF metering circuit contained on circuit card A4. One signal is tapped from the AF GAIN control input and the second signal from the monitor output

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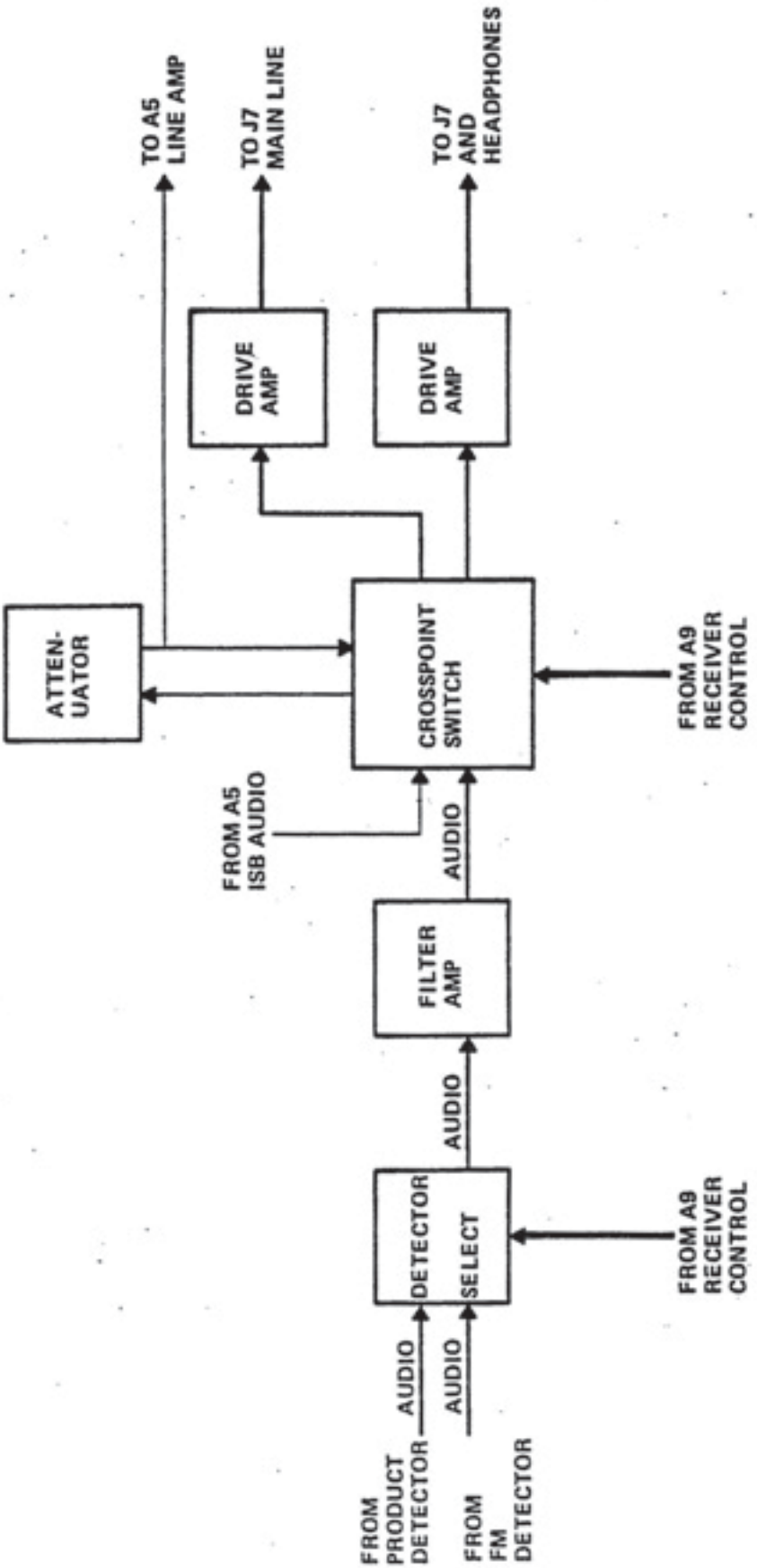

Figure 4-6. A4 AF Circuits Functional Block Diagram

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amplifier. These two signals are connected to transistor gate U19C which selects between the two signals on direction from Receiver control. In all modes except BITE the signal from the monitor output amplifier is selected and routed to the AF metering circuit. This circuit is described under AGC circuits.

4.3.4.3 AGC Control Circuits

Figure 4-7 illustrates a functional block diagram of the AGC circuitry contained on circuit card assembly A4. The circuits consist of an AGC detector, AGC decay, peak signal detector, decay time constants, an integrator, filter, a gain control distribution amplifier, a digital to analog converter and various electronic switches controlled from receiver control circuits. The description also includes the AF/RF meter comparator circuit.

The AGC circuitry is designed to provide three modes or techniques for controlling the gain of the Receiver; Manual, Automatic and Automatic with a selectable threshold. In the automatic mode the level of the IF amplifier U8 is controlled automatically with three selectable decay times; SHORT, MEDIUM and LONG. In the manual mode the IF GAIN control is used to control the level of the AGC signal applied to the IF amplifier U8. The IF GAIN control is used to select the threshold in the automatic with selectable threshold mode. The same decay times as in automatic are selectable in this mode.

An IF signal taken from IF emitter follower Q6 is coupled through capacitor C31 to U10A for detection. The three transistor array U10 acts as a detector to the IF signal with U10C connected as an emitter for buffering the DC signal to two circuits; AGC decay and peak signal amplifier. Peak signal amplifier U7C couples the signal, across a decay time select circuit, to integrator amplifier U14A. The signal routed to the hang circuit which consists of amplifier U7A and U7B is time controlled through capacitor C42, resistors R45 and R146 and transistors Q2 and Q10. When short time decay is selected, Receiver control turns on transistor Q2 and transistor gate U12A. Capacitor C42 is shorted to ground through transistor Q2 which turns on transistor U10D and a short delay is asserted using combination resistors R52 and R55. When medium time decay is selected transistor Q10 and transistor gate U11Ais asserted. Capacitor C42 discharges through the parallel resistance of R45 and R146 providing a short hang time, after which U10 is turned on and a medium delay is asserted through R52 and R53. When long time decay is selected capacitor C42 discharges through R45 providing a long hang time, after which U10 is turned on, decay time is through R52.

The AGC applied to integrator amplifier U14A is mixed with signals from diversity AGC through amplifier U14B and gain control or threshold from amplifier U14C when AGC mode dictates. In the manual mode both transistor gates U11C and U12B are enabled through receiver control and the gain control voltage is asserted directly to the input of U14A. In the manual with automatic threshold mode U12B is turned off and the voltage from the IF GAIN control asserts itself through diode CR20 only when that level is higher than the AGC signal at the input of U14A. The digital to analog converter is coupled through U11D and is used to insert threshold level from a remote location through receiver control. Diversity AGC applied through transistor gate U11C to the input of U14C and to amplifier U14B influences the AGC signal only when its level is higher. When AGC dump is enabled (during certain BITE modes and local/remote operations that require dumping of AGC) receiver control enables flip-flop U9A which turns on transistor U10E. This rapidly discharges capacitor C52 thereby preventing U14A from acting as integrator.

The integrator amplifier is coupled to AGC filtering; consisting of capacitor C59, resistors R76, R77, R81 and R83, diode CR21 and amplifier U17A. If AGC dump is asserted (in certain BITE modes) transistor gate U12D is turned on providing a much faster charge patch for C59 through resistor R78. The output of the filter amplifier U17A is coupled to amplifier U17B. This amplifier provides the AGC signal to IF amplifier U8. At the same time U17B provides one input to A3 AGC drive amplifier U17D through diode CR26. If ISB is installed and enabled a second AGC signal

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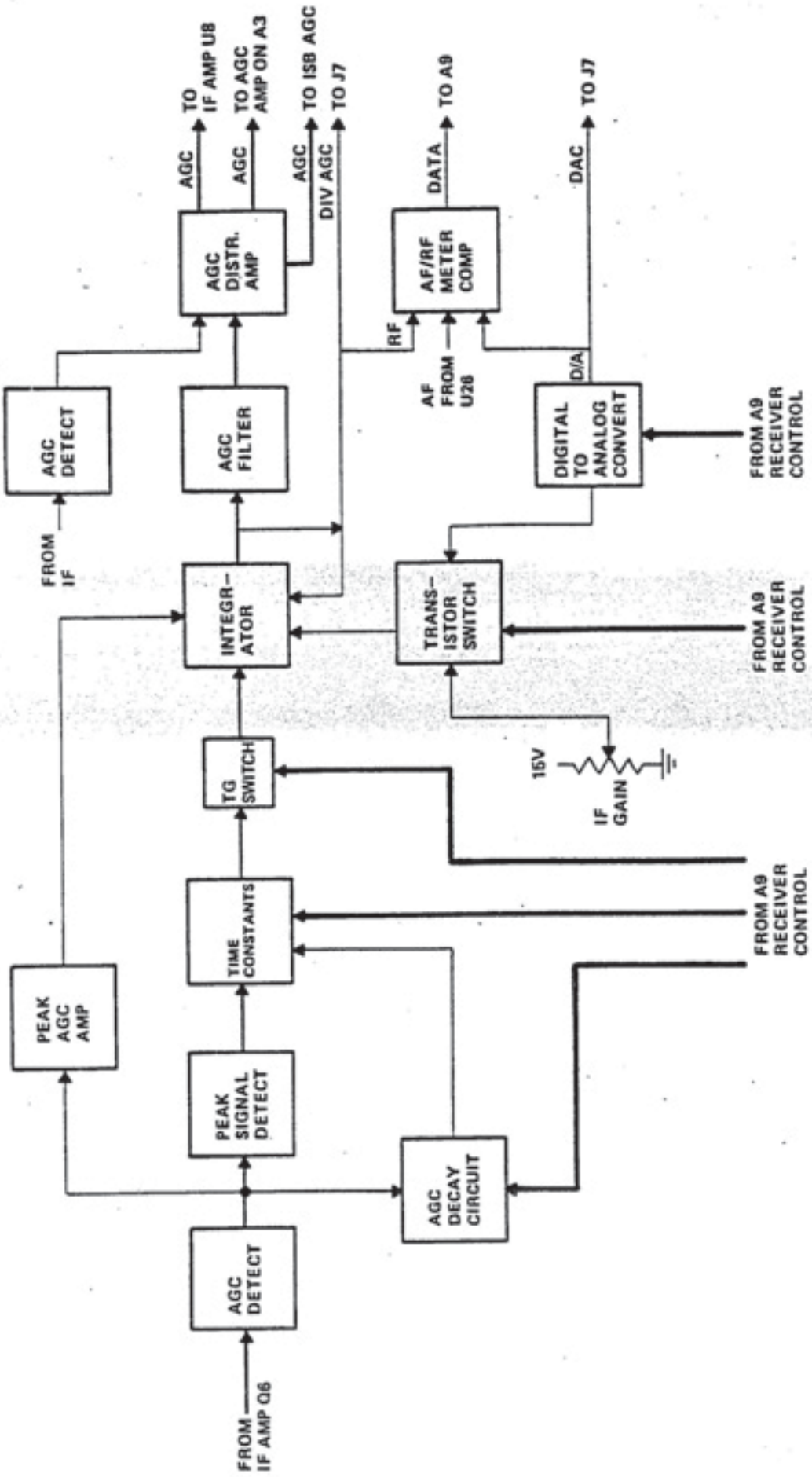

Figure 4-7. A4 AGC Circuits Functional Block Diagram

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from that circuit card is coupled to U17D through diode CR27. The two diodes biases the strongest of the two signals to the input of U17D. The output of this amplifier is coupled through J2 to AGC circuits on circuit card assembly A3.

An AF/RF meter comparator circuit is contained on circuit card assembly A4. This circuit monitors the main RF, the ISB RF and the AF that may be input from either the main or the ISB signal. The circuits consist mainly of comparator amplifiers U24A (AF), U24B (ISB-RF) and U24C (main-RF). All three amplifiers operate in the same manner with their negative inputs accepting the AF or RF reference while the positive input is referenced from the digital to analog converter U21. The output of each amplifier is output through connector J2 to Receiver control. From this information the microprocessor adjusts the input to U21 which in turn adjusts the converter signal to the AGC in all modes except manual. The output of the three comparators are also processed to the front panel meter readout where the RF or AF signal level can be monitored.

4.3.5 Independent Sideband (ISB), A5

The Independent Sideband (ISB) circuit card assembly A5 contains IF circuits, AF circuits and AGC circuits. The description of these basic circuits are divided into those three basic functions and shown in two separate functional block diagrams in Figures 4-7 and 4-8. Input signals to the circuit card include; IF signal, BFO signal, AGC, and audio signals from A4. Output signals include; AGC and audio to A4, and AGC and audio to AF OUT-J3 on the rear panel, but through circuit card assembly A4. The ISB circuit card assembly schematic diagram is shown in Figure 7-5.

4.3.5.1 IF Circuits

Figure 4-8 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4 along with the AF function. This circuitry consists of a four stage IF amplifier, a BFO amplifier, a product detector, an audio amplifier, two audio line drive amplifiers, and AGC circuits. The IF signal is routed from bandpass filter FL1 by the filter selection switch, located on circuit card assembly A4 to the IF amplifier on A5. This filter is selected in the ISB mode of operation, so that an IF signal is routed to A5 only in that mode. The IF amplifier is identical to the one located on A4 and is described in Paragraph 4.3.4.1. The IF signal from the AGC controlled IF amplifier is routed both to the AGC circuits and to the signal input port of a product detector U11. A BFO signal from A4 is applied to the base of transistor Q7 through capacitor C30, amplified and applied to the carrier input port of the same detector. The detector removes the carrier and applies, through its audio output port, the audio signal, through capacitor C43, to an audio amplifier.

4.3.5.2 AF Circuits

Figure 4-8 shows a functional block diagram of the AF circuitry, along with the IF circuits, as they function on circuit card assembly A5. This circuitry consists of an audio amplifier and two audio line driver amplifiers. The audio signal, as received from the product detector, is connected, through capacitor C43 and resistors R78 and R79, to the base of emitter follower amplifier Q8. The output of this amplifier is then routed to circuit card assembly A4. Refer to 4.3.4.2 for a description of the ISB audio on A4. The attenuated audio signal is routed back to A5 and applied to the input of one line driver amplifier integrated in U12. The output of this amplifier drives transformer T2 with a center tapped 600 ohm output. This output is routed to AF OUT-J3 on the rear panel. The main audio signal from the A4 audio is connected to the second amplifier U12 and processed in the same manner as the ISB audio except through transformer T1.

4.3.5.3 AGC Circuits

Figure 4-7 shows a functional block diagram of the AGC circuits for circuit card assembly A4. These circuits are identical to ISB AGC circuits and are described in Paragraph 4.3.4.3.

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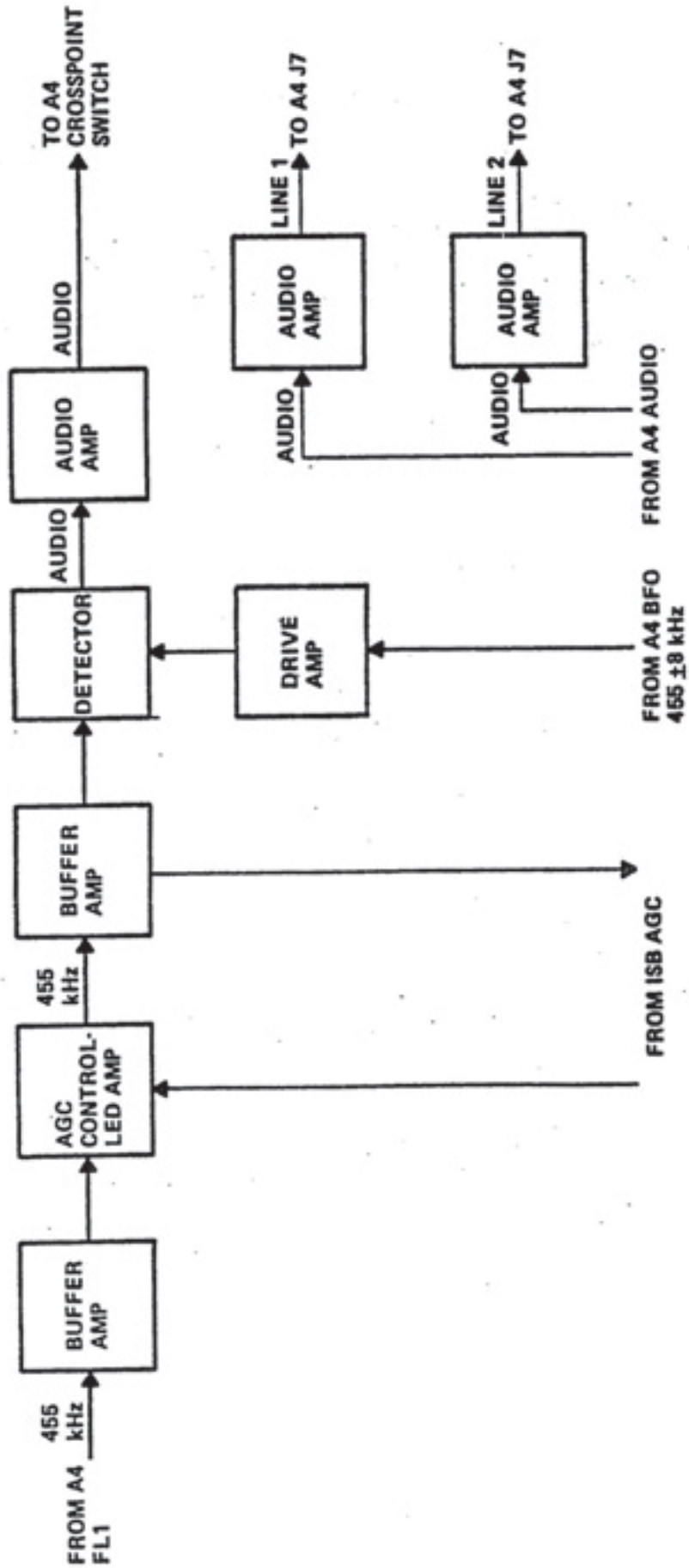

Figure 4-8. ISB Functional Block Diagram

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4.3.6 First Local Oscillator Synthesizer, A7

The first local oscillator synthesizer circuit card assembly A7 contains circuits to produce the first oscillator frequency of 40.955 to 70.454999 MHz for the first mixer which in turn produces the first IF signal of 40.455 MHz. The description of this circuitry is divided into three basic groups: operation of phase lock loops, the digital control circuitry and the oscillator control circuitry. Figures 4-9 through 4-11 respectively, show simplified block diagrams of the three basic circuit divisions. Input signals to the circuit card assembly include receiver control and a 1 MHz reference frequency. The only output signal from the assembly is the 40.955 to 70.454999 MHz oscillator signal.

4.3.6.1 Operation of Phase Lock Loops

A basic phase lock loop consists of essentially four main blocks. These are shown in Figure 4-9 and are a Voltage Controlled Oscillator (VCO), a divider capable of dividing the output of the VCO by an integer number (÷N), a phase detector (Ø) and a Loop Filter Amplifier (LFA). A phase lock loop configured in this manner is capable of locking to the incoming reference frequency (F ref) and in discrete steps, each frequency step being the same as the incoming reference frequency (F ref). This is derived from the fundamental formula for this type of loop which is Fo = F ref x N; therefore, to vary the main VCO Frequency (Fo) either Freq or N would have to be changed. Most loops perform frequency change by modification of N, the integer divide ratio. It is noted, however, that this type of simple single loop can only vary in frequency steps as small as the reference frequency (F ref). However, it is assumed that a system is possible whereby the main oscillator (Fo) frequency can effectively divide a fractional number, then it is possible to achieve a much finer resolution given the same higher frequency reference. Assume that Fo is 50.123467 MHz and the reference frequency is 100 kHz, then using the above formula the result is with n as the ratio, a non-integer number: 50.123467 = 0.1 x n; therefore, n = 501.23467. If we split this number into its integer part and its decimal part, the result is a three decade integer and a five-decade decimal number. Generating the non-integer part as an actual frequency is done by considering a portion of the frequency spectrum of interest between 50.1 MHz and 50.2 MHz where this finally generated frequency will occur. Thus, it is possible to generate any signal between these two frequencies by an averaging technique, that is to say (see Figure 4-12) if the signal at 50.2 MHz is sampled, 23,467 times and the signal at 50.1 MHz, 76,533 (100,000-23,467) times then the average or apparent signal produced by this sampling would occur at the frequency of interest at 50.123467 MHz. This type of sampling produces a large number of sampling sidebands on the main output frequency. These can be removed, however, by producing a signal equal and opposite to these predictable sidebands and adding this to the oscillator control signal and effectively nullifying the production of these sidebands.

In the synthesizer used in the receiver the circuitry can be split into two; for the operating analysis, those circuits involved in the generation of the digital signals to control the generation of the 5-decade decimal part of the divide ratio number (n) which in turn controls the sampling technique and the signal to sum with the oscillator control signal, and those circuits including an oscillator, 3-decade integer divider, phase detector, summing amplifier and lowpass filter making up the components of a simple phase lock loop. These two parts in further discussions will be referred to as the Digital Control and the Oscillator Control circuitry. A separate section is included for auxiliary circuitry which is provided to produce large frequency step control and out-of-lock indications for the receiver.

4.3.6.2 Digital Control

Figure 4-10 illustrates a simplified block diagram of the digital control circuitry. The circuitry associated with the time control, the incoming 1 MHz reference signal from A7J2, is used as the clock for accumulator and registers through the NOR gate U4D which drives U20, U21 and

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NOTE:
FOR NORMAL OPERATION
$f_o = f_r \times N$
WHERE:
f_o = OSCILLATOR FREQUENCY
f_r = REFERENCE FREQUENCY
N = DIVIDE BY NUMBER

Figure 4-9. Typical Phase Lock Loop Functional Block Diagram.

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U22, and is routed directly to U3, U5 and U18. The Hex D flip-flops U3 and U5 with U1A and U1B provide a 10-level, ring counter. This counter is used to provide timed pulses to clock the accumulator from first accumulation to second accumulation and sequentially clock out the data in the latches U8 through U12 to the full adder U15. Flip-flop U3 provides a pulse 1 clock pulse wide but delayed 5 pulses from DØ the input, to Q1 the output. The output at U3Q4 is connected to the input DØ of U5. U5 also provides 1 clock pulse wide pulses but each output QØ through Q4 is used to drive the incoming data latches. U4A and U4B convert the narrow pulses from U3 QØ and U5 QØ into a 50% duty cycle square wave with a period of 10 clock pulses (each half cycle 5 clock pulses long). The 180° out-of-phase outputs at U4A pin 1 and U4B pin 4 provide control to U2, U22 and U19 to ensure that these devices are enabled during the correct half cycle. The 100 kHz reference for the reference side of the phase comparator is taken from U5 output Q4. U5 output QØ is provided to U4C via U7C to reclock the CARRY IN to U15 and also to U6 to provide the clock for alignment of signals out of the HEX D flip-flop U6.

In serial-to-parallel conversion, the incoming serial data stream from the A9 Receiver control assembly consists of DATA, CLOCK and STROBE signals. The strobe is routed to U6 input D1 where its output is reclocked. This output at U6 Q1 is fed back to D2 and its output Q2 provides a strobe input to U13 and U14 one clock pulse delayed. The incoming CLOCK is fed to U14 through U8 in parallel. The serial DATA is fed first into U14 which from its output on U14 pin 10 to U12 and U13 shift registers. The output from U12 at pin 10 is fed to U10 and U11, and so on to U9 and U8 to complete the data load and forming the serial-to-parallel conversion of synthesizer data into the data registers. The data registers U8 through U14 hold the data for the synthesizer frequency, the U8 register holding the 4-bit BCD data for the 1 Hz digit and each register the next decade so the U9 register holds the 10 Hz data and so on to the U14 register which holds the 1 MHz and 10 MHz data.

If the front panel RF frequency is set to 10.426800 MHz then the actual loaded data is 39.255 MHz above this frequency which is 49.680800. The first IF frequency is 40.455 MHz so we can see that a further offset of 1.2 MHz less than the main LO frequency of 50.881800 is introduced by the microcomputer into the serial data stream sent to A7. This is accounted for in the actual mathematical process in the first and second accumulator circuitry, which replaces this offset before generating the final VCO control voltage to the local oscillator

With accumulator operation, the data loaded into the registers U8 through U12 is fed in 4 parallel boards under control of the ring counter U5 during the first half cycle of the tuning as discussed in the tuning section to the Full NBCD Adder U15. As the accumulation proceeds, the accumulating sum is passed from the sum outputs of U15 to the 4-bit wide latch U18. The Carry Out signal from U15 is also stored in U18 and is clocked out to U7A and then under control of U7C from the tuning circuits through U4C back into the Carry-In port of U15 deriving the first accumulation the outputs from U18 will be propagated through into the 4 stage shift registers contained in U20 and U21. U20 and U21 are 18 stage registers divided each into 2 four stage registers and 2 five stage registers. The four outputs from U18 are fed into the 4-stage registers in each half of each U20 and U21 and then the output of these 4-stage registers is fed back to the 5-stage register in each half of U20 and U21 At the end of the first accumulation the data at the output of the 4-stage register appears at the input to the tri-state 4-bit buffer U2A.

As the second accumulation begins U2A is enabled, under control of U4A, and the data at its inputs is transferred to the B inputs of U15 the NBCD Adder. During the five clock periods of the second accumulation the data in U20 and U21 is shifted back to the B inputs of U15. During this period, the data in U8 through U12 is held as the tri-state output enable of these registers is not enabled ensuring the results of the first accumulation is added again in the second accumulation. At the end of the second accumulation the results of the first accumulation will be propagated through the 5-stage register in each half of U20 and U21 and will appear at the inputs DØ through D3 of the

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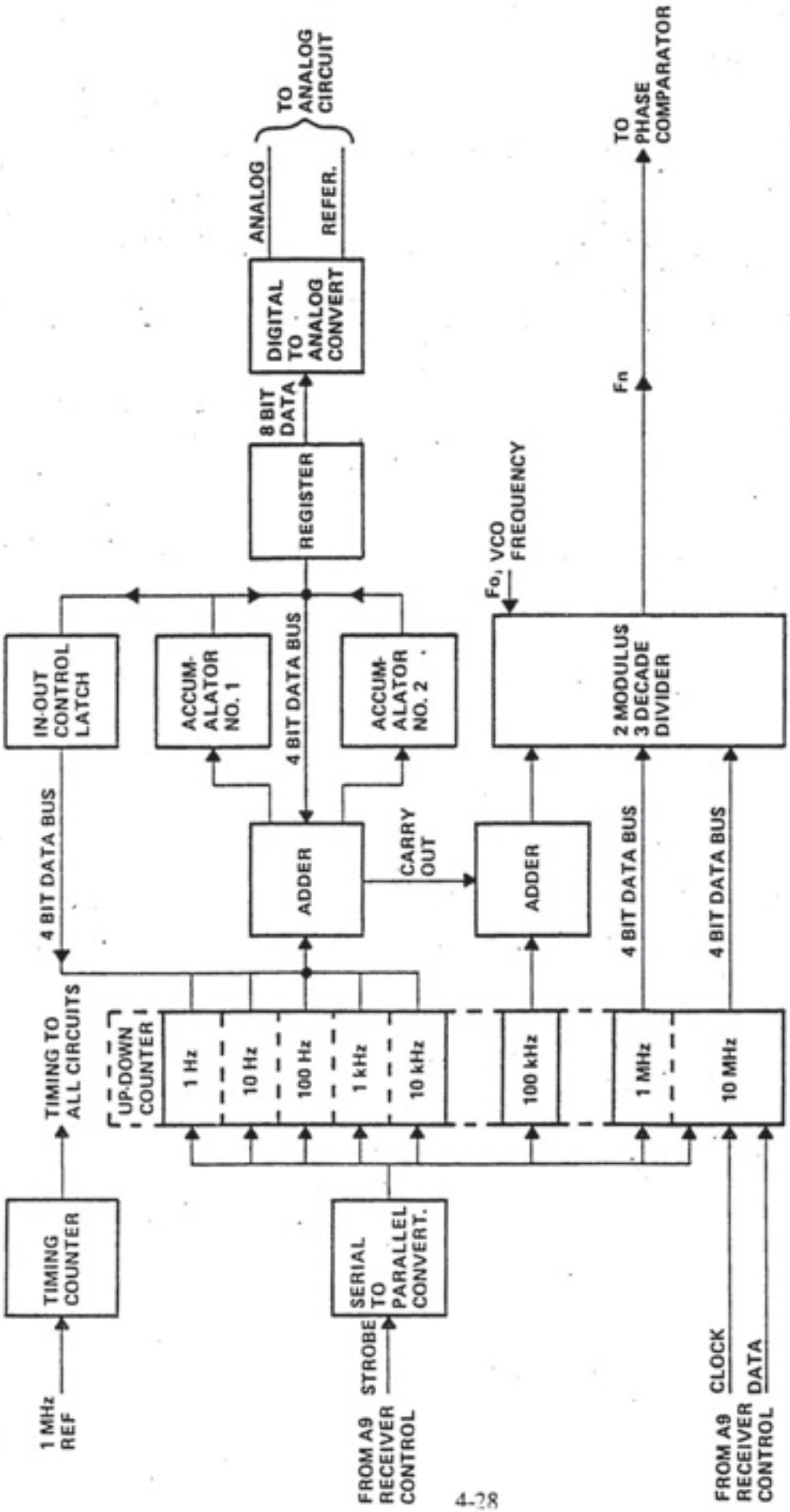

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Figure 4-10. First Local Oscillator Digital Circuits Functional Block Diagram

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4 x 4 Multiport Register U22, and at the A1 through A8 inputs to U15. If no new data is loaded into U8 through U12 from the serial input data stream, then the two cycles of accumulation will continue; first accumulating the contents of U8 through U12 on one half cycle with the data at A1 through A8 in U15, and on the second half cycle adding the results from the first accumulation back into the B inputs of U15. Temporary storage for the results of each accumulation is provided by U18, U20 and U21.

If the result of adding numbers in U15 is a terminal count, the adder will produce a Carry-Out pulse at U15 pin 6 and reset to zero and start counting again. In a real situation this process is on going and the adder is continually providing Carry-Out pulses. (See Figure 4-12, line B.) This Carry-Out pulse is fed to U6 to be reclocked. The reclocked output at U6 pin 7 is routed through U1C to a further adder U17. The carry out is also clocked by U19A so that if it occurs on one edge of the accumulating half cycle controlled from U4B, it will appear at the Q output of U19A and after reclocking in U6 through the fifth latch it is applied to the carry input of the 4-bit full adder U17. (See Figure 4-12, line C.) The adder U17 continually updates,by addition, based on the carry out information from U15, the 100 kHz frequency information, provided by the input storage register U13. The addition in this adder is continuous so that the outputs at U17 pins 10 through 13 are constantly changing to provide the averaging action previously discussed.

For DAC control, a 4 x 4 multiport register U22 provides storage for the results of the constant accumulations and provides the information to the digital-to-analog converter U23. U19B divides the accumulator control signal by two so that all four registers in U22 can be loaded. The read cycles to these registers are controlled by the RØA, RØB, R1A and R1B inputs of U22. The RØA and RØB inputs are fixed and the R1A and R1B inputs are controlled by the output of U19B so that during two accumulations R1 is loaded, each register RØ and R1 consisting of two 4-bit data storage areas. The data stored is that which appears at the data inputs of U22, DØ through D3. This stored information is transferred to the register A outputs and register B outputs when W Enable is high and either WØ is high transferring RØA and RØB contents or W1 is high transferring the contents of R1A and R1B.

The digital-to-analog converter provides an output based on the changing data at its inputs as a voltage ramp whose amplitude and DC offset is modified by the adjustment of R5. The D/A also provides a reference source for the pulse to voltage converter U33.

NOTE

The pulses demonstrated in Figure 4-12 can be reproduced in circuit if the RF front panel frequency is set to 1.046000 MHz and the test points TP1 and TP2 temporarily shorted. This ensures that the accumulations start from a zero condition. B will then be at TP3, C at TP4 and E at U23, pin 2 (the D/A output).

4.3.6.3 Oscillator Control

Figure 4-11 presents a simplified block diagram of the oscillator control circuits. To more fully understand the operation, the following description is divided into four principal areas; 1) Main Division, 2) Phase Comparator and Pulse-to-Voltage Converter, 3) VCO and Analog Control Circuitry, and 4) Speed-Up and Out-of-Lock Operation:

1. Main Division. The BCD data outputs for 100 kHz, 1 MHz and 10 MHz provided by U17 and U14 are applied to a 2-modulus, 3-decade divider consisting of U27, U29, U30 and U31. This form of division ensures that by using a 2-modulus high speed control device U27 that can divide by 10 or 11 under control of its M1 and M2 input control can divide a high frequency input by an

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Figure 4-11. First Local Oscillator Analog Circuits Functional Block Diagram

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integer value. The terminal count from U29 is applied inverted by Q5 to this control input of U27. The resultant divided signal at pin 9 of U29, U30 and U31 is applied to a TTL to ECL converter network consisting of R30, R31 and CR7 to a flip-flop U28A. This flip-flop reclocks the divided output under control of the clock signal on U28A pin 6 from the ECL output U27 pin 8, and then applied to one side of the phase comparator from its quadrature outputs on pins 2 and 3.

2. Phase Comparator and Pulse-to-Voltage Converter. The phase comparator reference is derived from the 100 kHz signal from U5 pin 12, reclocked against the 1 MHz reference in U26A. The reference output at U26A pin 2 is applied to the other side of the phase comparator consisting of U28B, U26B and U32. The ECL comparator provides phase comparator outputs at TP7 and TP8. The variable input from U28A pin is applied to a pulse-width detector consisting of CR9, CR10, Q6 and U33B. As the pulse width changes as the frequency varies from 40.455 MHz to 70.454999 MHz the voltage at the emitter of Q6 varies continuously and linearly over a range of approximately 1 volt. The DC offset of this voltage is determined by the D/A ref from U23. U33A and Q8 from one-half of a current source to CR12 and CR14 and Q7 and Q9 from the bottom half of this current drive through CR13 and CR15. Phase compared outputs at TP7 and TP8 are fed into the diode network formed by CR12, CR13, CR14 and CR15 and an output from this pulse-to-current converter is fed to R60.

3. VCO and Analog Control Circuitry. The current output of the phase comparator is combined with the voltage ramp from the D/A through C80. This combined signal is then applied to an integrating amplifier U35. In normal operation, the output of U35 is sent to a signal linearizing/ inverter circuit U37A and to the out-of-lock window detector comprising U34C and U34D. This is described in more detail in the speed-up and out-of-lock circuit operation. The output of U37A at TP10 is a DC voltage that can vary from a high voltage up to 18 volts and a low voltage equal to 1 volt, it will be high voltage when the selected frequency is at 30 MHz and low when the system requires 0.5 MHz. This DC voltage is then passed through U37B which along with its associated resistors and capacitors forms a low-pass filter. This output is then buffered from the VCO by 120K resistor R88 between TP11 and TP12. A further lead-lag network is then in the VCO control line between TP12 and ground formed by R92, R93, R94 and C98. This voltage is then applied to the VCO control varactors CR3 and CR4 through R85 and L4. A voltage applied to CR3 and CR4 will vary the capacitance across the main VCO coil L5 and thus vary the frequency generated. Q1 is the main LO active device and an output from its drain is capacitively coupled to a buffer amplifier of the cascade type formed by Q12 and Q13. The output of this feeds the 2-modulus divider controller U27. A further output from the oscillator coil is tapped off and provides the main LO output through Q2 and Q3 with step down transformer T1.

4. Speed-Up and Out-of-Lock Operation. When a large step of frequency is introduced on the front panel or from remote the window detector U34C and U34D comparators, compares the inputs on pins 9 and 10 from the VCO control circuitry with fixed high and low references on pins 11 and 8. If the voltage goes higher or lower (frequency step up or down) than these references a pulse will appear at the comparator outputs on pins 13 and 14. This pulse is applied through an RC network to a voltage converter consisting of U34B and CR19 and CR20. This voltage off set pulse is then used to drive three switches U36B, U36C and U36D. These switches by- pass the lowpass filter U37B and increase the integrating bandwidth of U35 and one switch, provides a feed forward from TP10 to the positive input of U40. U40 provides an integrated drive to push-pull drivers Q10 and Q11, the action of these drivers is to high-speed charge or discharge C98 through R91, C97 and R94. When the control voltage is at approximately the correct voltage for the frequency selected this circuit becomes operative. U34A provides the Out-of-Lock signal for feeding to the A9 Receiver control board and then to A6A2 for processing. If a pulse or a constant low level is applied to pin 6 of U34A then its output will go low indicating OOL.

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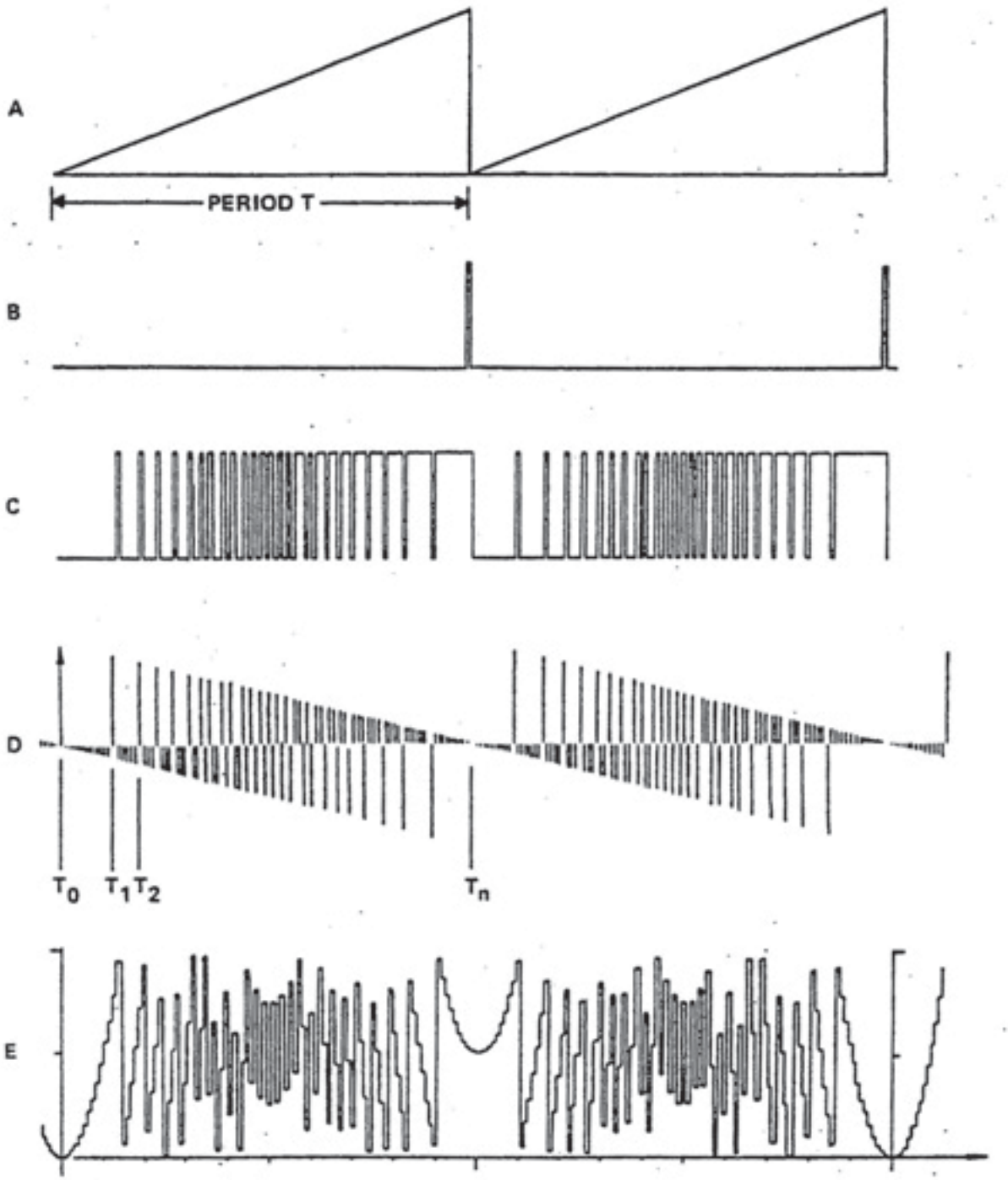

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Figure 4-12. Detailed Timing Diagram

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4.3.7 Second LO and BFO Generator A8

The second local oscillator and beat frequency oscillator circuit card assembly contains the circuitry for these two oscillators. An internal/external frequency reference circuit is also contained on this circuit card. The second local oscillator develops the fixed 40 MHz signals for the second mixer that in turn provides the 455 kHz second IF signal. The BFO is a variable oscillator that provides both the 455 kHz second IF signal and the basic 455 kHz beat frequency for sideband and CW modes of operation. The oscillator, through receiver control, may be either set at 455 kHz or varied plus or minus 8 kHz either side of its basic frequency for CW operation. The internal/external frequency reference circuit provides a reference frequency for both oscillators phase lock loops as well as the first LO contained on A7. In addition, the circuit includes an internal temperature controlled crystal oscillator which supplies a selectable 1 MHz, 5 MHz or 10 MHz reference frequency output at the rear panel. An external reference frequency can be used in place of the internal reference. The circuit description for the internal/external reference, the second LO and BFO are described under their respective headings with functional block diagrams shown in Figures 4-13 and 4-15. Schematic diagrams of these circuits are shown in Figure 7-10.

4.3.7.1 Internal/External Reference Frequency

The A8 circuit card contains circuitry that permits either an internal or external reference frequency. This reference frequency is required for the operation of all three oscillator synthesizers. A reference in/out connector and switch on the rear panel in addition to linkage on the A8 circuit card provide for the selection of either internal or external frequency and for selecting the proper divide by N frequency for the Phase Comparator.

4.3.7.2 Internal Mode

A 5 MHz crystal oscillator Y1, located on A8 is used as the internal reference frequency. With the rear panel REF INT/EXT switch in the INT position, the base of Q1 is grounded through R7 which turns voltage regulator U1 on. The voltage from this regulator enables the temperature controlled crystal oscillator. Approximately 30 minutes are required for maximum stability. The oscillator output is coupled through capacitor C5 to the base of transistor switch Q5. With the ground applied through the INT/EXT switch, the base of Q5 is held high through inverter U2A and diode CR3 while the base of transistor switch Q4 is held low through diode CR2. Transistor Q5 conducts, transferring the 5 MHz signal through a TTL square wave shaper Q6 to one clock input of the phase comparator. See 4.3.7.4, item 3. The 20 MHz voltage controlled oscillator, described in 4.3.7.4, item 2, is stabilized through the use of this reference frequency. The 20 MHz output of the oscillator is divided by three dividers (two ÷2, U7B + U7A and a ÷10, U6). The two dividers (÷2) are contained in a single dual D flip-flop. The clock signal (20 MHz) is applied to the clock input of U7A. With the Q output connected to the D input, the Q output provides the 10 MHz reference. The 10 MHz is also connected to the clock input of the second flip-flop and to the divide by 10 circuit. The second flip-flops Q output provides the 5 MHz reference signal. The divide by 10 circuit is a two stage divider (÷2 and ÷5). The 10 MHz drives the clock input for the divide by 5 at B input pin 1. The output of this divider (QD pin 11) is connected back to the clock of the second divider (÷2) at A input pin 14. Dividing by 5 first then by 2 provides a more symmetrical 1 MHz reference. The 1 MHz signal is output from the divider (÷2) at QA output pin 12. The 1 MHz, 5 MHz and 10 MHz frequencies derived from these dividers are available for reference through data select switches U4 and U5. The 1 MHz reference is routed directly to the BFO synthesizer and to the first local oscillator synthesizer through NAND gate U11C and connector J2. One of the three frequencies will be selected by data select U5 and routed to rear panel connector J7. Either one of the three frequencies may be selected by proper connection of links LK1 and LK2. In this internal mode, data select C of both U4 and U5 is held low through the INT/EXT switch. Linking LK1 makes data

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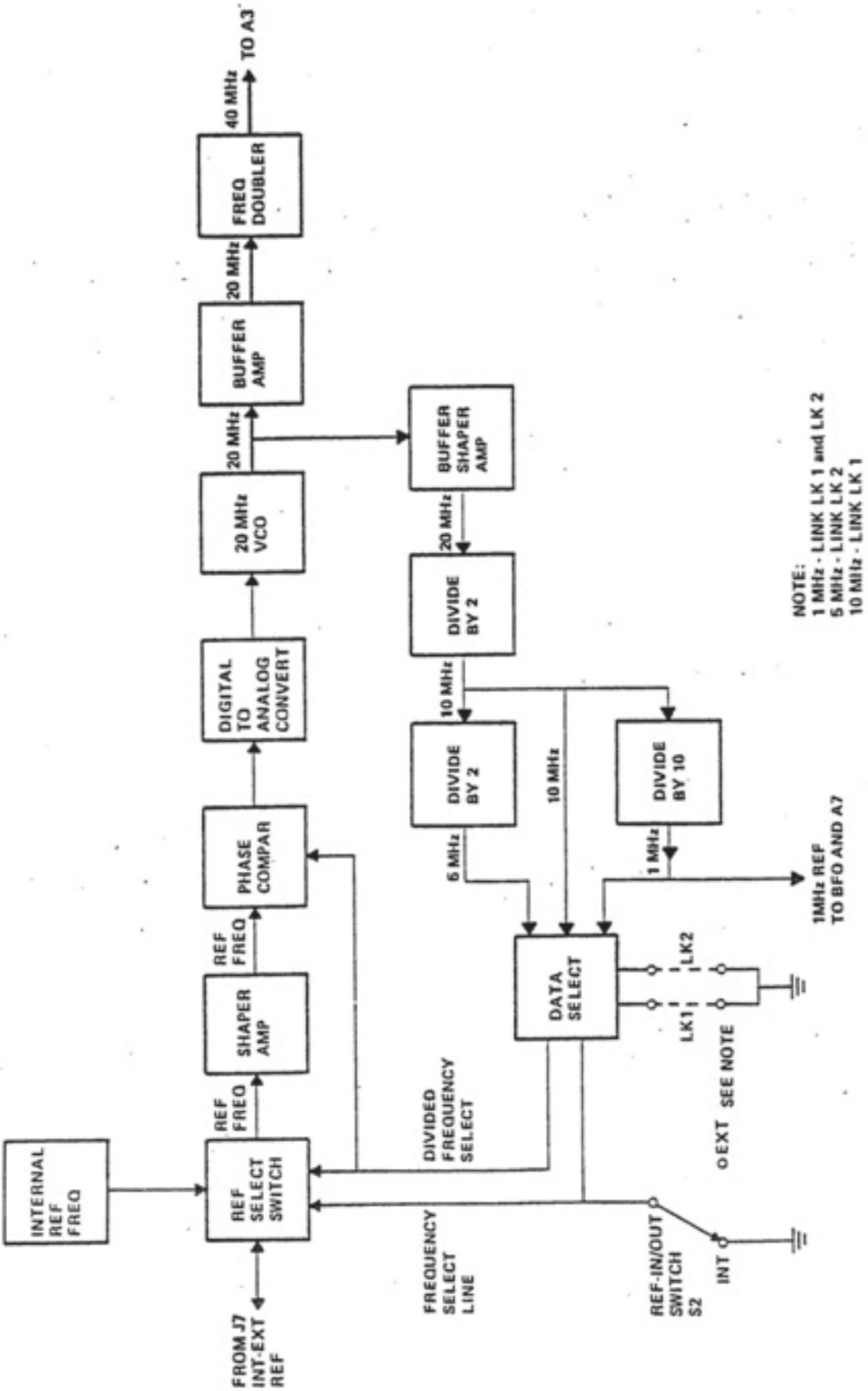

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Figure 4-13. Second Local Oscillator Fun tal Block Diagram

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select A low which outputs D0 input of both U4 and U5 to their respective Y outputs. For U4 this is 5 MHz, for U5 it is 1 MHz. When only LK2 is linked data select A will be high and B low which connects both D1 inputs to their respective Y outputs (U4-5 MHz, U5-5 MHz). When both LK1 and LK2 is linked both data select A and B are held low which outputs D3 of both U4 and U5 (U4-5 MHz, U5-10MHz). As noted in this internal mode, U4 always selects the 5 MHz. It is then routed to the phase comparator as the oscillator reference signal. The output frequency selected by U5 is routed through resistor R13 to buffer amplifier stages Q3 and Q2. These stages provide for output into 50 ohms through a high pass filter, L1, C6 and C7, and connector J7 on the rear panel. The high pass filter also provides filtering for reference frequencies applied externally through J7 while resistors R8 and R9 provide a 50 ohm impedance to the incoming reference frequency.

4.3.7.3 External Mode

In this mode of operation the INT/EXT switch is set to EXT and this line goes high from the +5 volts through resistor R78. This causes transistor Q1 to turn voltage regulator U1 off which in turn turns off the internal crystal oscillator Y1. When an external oscillator is connected to connector J7 on the rear panel, the input is routed through the high pass filter, and capacitor C8 to the base of transistor switch Q4. The input of NOR gate U2A is now high which in turn keeps the base of Q5 low through diode CR3. Transistor Q4, whose base is no longer low, conducts which applies the external reference through the TTL shaper to the same clock input of the phase comparator that the 5 MHz reference was applied in the internal mode. The appropriate reference frequency for application to the second clock input to the phase comparator can be selected through LK1 and LK2 as in the internal mode; however, data select C is now high. Linking LK1 selects D6 (10 MHz), LK2 selects D5 (5 MHz) or both LK1 and LK2 select D4 (1 MHz). The D0, D1, and D2 inputs to U5 cannot be selected when data select C is high (external mode) and no output appears on the Y output of U5.

4.3.7.4 Second Local Oscillator

Figure 4-13 shows a simplified functional block diagram of the second local oscillator. The circuit consists mainly of a crystal referenced, voltage controlled oscillator, a frequency doubler output circuit and a phase lock loop includes amplifiers, an ECL to TTL buffer, three frequency dividers (two ÷ 2 and a ÷10), reference frequency select circuit, a phase comparator and a digital to analog converter. The three dividers are used to provide a choice of reference frequencies for internal or external reference.

1. Phase Lock Loop. The 20 MHz oscillator frequency is kept on frequency through a phase locked loop (See Figure 4-9). The oscillator output is routed through a divide by N circuit that provides an oscillator reference frequency. This divided oscillator frequency is coupled to the second clock input of a phase comparator. The phase comparator, described below, detects any phase shift between the oscillator frequency and a reference frequency also connected to the phase comparator. The phase comparator then changes the digital to analog converter output voltage which is connected to the oscillator varactor and crystal. This then causes the oscillator frequency to change. This loop action will continue until the oscillator frequency is brought into phase (same frequency) with the reference frequency.

2. Voltage Controlled Oscillator. The 20 MHz oscillator consists of ECL OR gate U22D, 20 MHz crystal Y2, varactor CR4, resistors R47, R48, R49 and R50 and capacitors C34 through C38. Oscillation frequency is derived from the parallel combination of crystal Y2 in series with C37 and with varactor CR4 in series with C34. The dc voltage applied at the junction of CR4 and Y2 controls the reactance of the parallel circuit, mainly through CR4. This dc voltage, controlled

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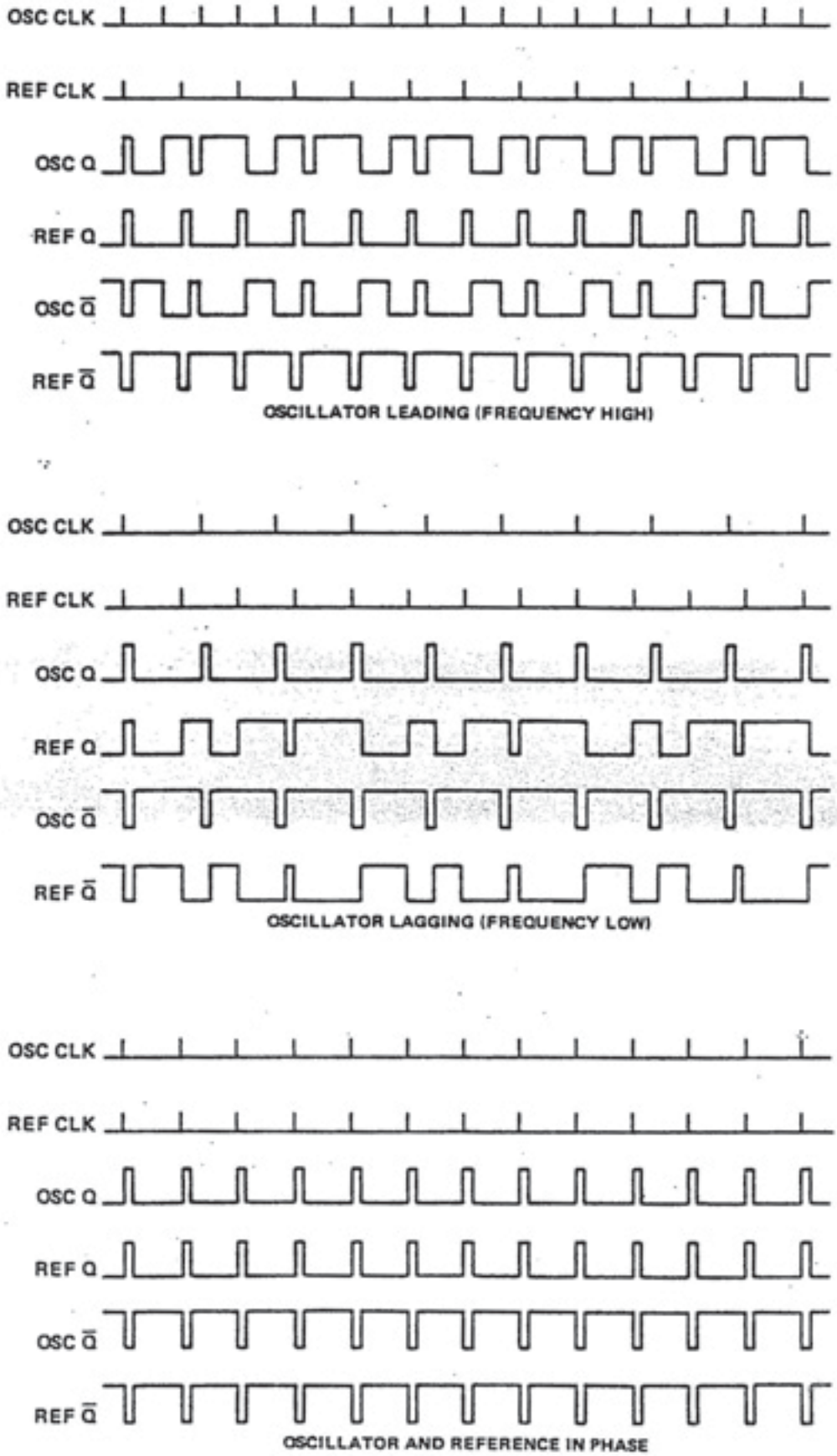

Figure 4-14. Waveform Diagram: Phase Comparator

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through the phase lock loop described in Paragraph (1) compensates for any frequency shift of the oscillator. The oscillator output is coupled to two buffer amplifiers U22A and U22B. Buffer U22A is used to drive a TTL shaper buffer amplifier, Q10, which shapes the oscillator output into a square wave for input to the divider. These circuits are described in Paragraph a. Buffer U22B drives a frequency doubler circuit, Q11, and associated components. This tuned circuit selects the 40 MHz component of the signal and outputs it through J3 to circuit card A3 as the second oscillator frequency.

3. Phase Comparator and Digital to Analog Converter. The phase comparator is used to detect the phase shift between the reference frequency and the oscillator frequency and to apply control to the digital to analog converter in relation to that phase shift. The comparator consists of dual flip-flop U3A and U3B and NAND gate U2B. Flip-flop U3A is clocked from the reference frequency while U3B is clocked from the divided oscillator frequency. The D inputs to both flip-flops are held high through the +5 volts. When both Q outputs are high the output of NAND gate U2B goes low, resetting both flip-flops with a delay through R32 and C20. Thus when the positive edge of a clock signal clocks a flip-flop, Q goes high while $\overline{Q}$ goes low. If the two clock signals to the flip-flops are in phase, the $\overline{Q}$ outputs then will go high from the reset action through NAND gate U2B, initiated from the leading edge of both clock pulses. The $\overline{Q}$ outputs will remain high through the on-off period of that particular clock pulse. Except for a small delay time introduced by the flip-flops the $\overline{Q}$ outputs will be high most of the time when the two clock signals are in phase. (See Figure 4-14). When the oscillator frequency leads the reference signal (frequency high), the $\overline{Q}$ output of U3B remains on less than the $\overline{Q}$ output of U3A because the leading pulse sets back to Q on U3B before the lagging pulse of the reference signal sets back to Q on U3A. The reverse of this is true when the oscillator frequency lags the reference signal (frequency low). The two $\overline{Q}$ outputs of the phase comparator are coupled to a digital to analog converter which consists of transistors Q7, Q8 and Q9, resistors R33 through R39 and capacitors C24 through C26. The $\overline{Q}$ output of reference flip-flop U3A is connected to the emitter of Q7 through R33 while the $\overline{Q}$ output of the oscillator flip-flop U3B is connected to the emitter of Q9 through R34. When the oscillator and reference signal are in phase, the two outputs are the same and transistors Q7 and Q9 conduct at a rate dependent on the amplitude and time period of the pulse. With the amplitude always constant, the amount of conduction then depends only on the time period. When the pulse goes high, the emitters of Q7 and Q9 go more positive causing them to conduct less and when the pulse goes low, they conduct more. The voltage output at the common collectors of Q8 and Q9 would tend to follow this rise and fall in the pulse; however, the inverted signal at the base of Q8 also causes it to conduct less when the pulse is high and more when the pulse goes low. This action converts the pulse signals into a dc level sawtooth waveform at the Q8-Q9 common collectors. The low pass filter, C25, C26 and R39 smooths this waveform and dampens sudden changes caused from changes in the phase comparator pulse rates and in turn stabilizes the phase lock loop. When oscillator frequency increases, the pulse rate increases, the pulse rate increases at Q7 and decreases at Q9, causing a reduction of the dc level output. When oscillator frequency decreases the reverse action takes place. This analog dc output is coupled through R47 to the oscillator for frequency control.

4. Out of Lock Detector. The out of lock (OOL) detector consists of NAND gate U2C, resistors R43 and R44 and capacitors C29 and C31. The NAND gate output is held low (phase loop in lock) by the $\overline{Q}$ outputs of the phase comparator. The resistor capacitor combinations R43-C29 and R44-C31 integrate the square wave signal to provide a constant high on the two NAND gate inputs. If either or both of the two $\overline{Q}$ outputs from the phase comparator remains low the output of the NAND gate will go high. The OOL output from this circuit is routed to A9 front panel control for processing.

4.3.7.5 Beat Frequency Oscillator (BFO)

Figure 4-15 is a simplified block diagram of the beat frequency oscillator. This circuit provides the variable 455 kHz BFO for receiver CW and sideband operation. The BFO is varied plus

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Figure 4-15. Block Functional Block Diagram

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or minus 8 kHz through receiver control. The oscillator operates in a phase locked loop which consists of a voltage controlled oscillator (VCO), a buffer amplifier, a programmed divider, a phase comparator and a digital to analog converter. A divide by 2000 circuit is included to provide a 500 Hz reference signal for the phase comparator. The VCO operates at a center frequency of 22.75 MHz which is 50 times the BFO center frequency of 455 kHz. The oscillator output is routed through a buffer amplifier, TTL shaper, divide by 50 circuit and filter to provide the 455 kHz BFO to the A4 circuit card. An out of lock (OOL) circuit is also included to detect any out of lock condition of the phase lock loop.

1. Phase Lock Loop. The phase lock loop for the BFO oscillator functions in the same way as the circuit described for the second local oscillator except the divide by N is made variable through BFO input data to the divide by N circuit.

2. Voltage Controlled Oscillator. The VCO consists of field effect transistor Q18 opto isolator U21, coils L4 and L5, resistors R66 and R67, capacitors C52 through C56 and C59 and varactors CR6 and CR7. The capacitive reactance of the two varactors in conjunctions with L4 determines the frequency at which the circuit will oscillate. Since varactors change capacitance in relation to the level of the dc voltage applied, the frequency of the oscillator is controlled from the output of the digital to analog converter that is applied to varactors CR6 and CR7 through coil L3. Opto isolator U21, connected to the source of Q18 through resistor R67, provides for on-off control of the oscillator by isolated control of the oscillator source bias. When BFO is enabled in the CW and sideband modes, U21 is enabled through pin 2 which in turn completes the bias path for Q18 through R67. The output of the oscillator is coupled through capacitor C57 to the gate of field effect transistor Q19 which acts as a buffer amplifier between the oscillator and two output circuits. One output of the buffer amplifier provides the oscillator reference frequency through capacitor C72 to the programmed dividers. This circuit is described in Paragraph 3. The second output is coupled through capacitor C60 to a shaper circuit, Q20, R72, R73, R74 and C61. This circuit shapes the waveform into a square-wave for the TTL logic of the divide by circuit U20. The dual decade counter U20 is externally strapped to provide a division of 50 on its QD output, pin 9. The variable 22.35 to 23.15 MHz oscillator signal is reduced in frequency by the division of 50 which provides the 447 to 463 kHz BFO. This output is filtered through the filter network consisting of C63, C64, C65, L6, R75, R76 and R77. This filter shapes the digital waveform from U20 into an approximate sine wave signal before being routed to circuit card A4 through connector J4.

3. Programmed Dividers. The programmed dividers determine the divide by N number by which the oscillator frequency will be divided for a variable reference to the phase comparator. The program dividers consist of presettable BCD decade counters U14 through U18, divide by 10 or 11 2-modulus controller U19, NOR gates U12A through U12D and AND gates U13A through U13C. The program divider has two reference inputs; the oscillator frequency coupled through C72 to the V reference and clock inputs of U19 at pins 15 and 16 and the BFO data control inputs to U15 through U18. It is the BFO data inputs in conjunction with U19 that sets the divide by N number for dividing the VCO frequency. To divide the 22.75 MHz to 500 Hz, for the second clock input to the phase comparator, would require a division of 45500. The five decade counters are externally strapped to count down from a maximum count of 100000 (99999 + 1). The actual data then that would be set on the BFO inputs would be 100000 – 45500 = 54500; however due to gating restrictions between the decade counters the actual number set at the BCD inputs is 54509 at center frequency (455 kHz). The BFO is adjustable plus or minus 8 kHz so that the swing in the BCD inputs must be from 53709 (54509 – 800) to 55309 (54509 + 800) with 54509 as center. At center frequency counter U18 receives the 10 Hz BCD digits on its parallel inputs P0 through P3 with P0 and P3 ($2^0 + 2^4 = 9$) high. Counter U17 receives the 100 Hz digits with all input low (0), U16 receives the 1 kHz digits with P0 and P2 ($2^0 + 2^2 = 5$) high, and U15 receives the 10 kHz digits with only P2 ($2^2 = 4$) high. Counter U14 is strapped P0 and P2 ($2^0 + 2^2 = 5$) to the +5 volts (high)

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and P1 and P3 to ground (low). This supplies the 100 kHz digit which is always 5. Counter U15 receives only the 2^0, 2^1 and 2^2 BCD digits since the 10 kHz swing is never greater than 7. The counter is a two modulus divide by 10 or 11 controller and will divide by 10 or 11 for different periods in the clock signal. The TC output of U18 coupled to the M1-M2 inputs of U19 determine the periods at which it will divide with either 10 or 11. NOR gate U12C ensures that the count enable input of U18 goes low when TC goes high. This assures that the TC output will be retained long enough for action on the M1-M2 inputs of U19. The QTTL output (pin 11) is used to clock the decade counters U14 through U18 and as a reclocking source for NOR gate U12A. Four control inputs, parallel enable (PE), count enable parallel (CEP), count enable trickle (CET) and reset (R) select the counters mode of operation. The R and CET of all counters is held high through the +5 volts connected to all counter CET and R inputs. The CEP input of counter U17 (100 Hz) is also held high from the same +5 volts since this counter does not receive a carry out from previous counters. The CEP of counter U16 is high only when the TC output of U17 is high, the CEP of U15 is high only when the TC output of both C16 and C17 through AND gate U13A are high and the CEP input of U14 is high only when the TC output of both U15 and U16 through AND gate U13B are high. This AND gating of the TC outputs help prevent extra pulses from occurring that are caused from delays in the counters. The PE of all counters are alternately low and high as the TC output to inverter U12B is alternately high and low. With the R and CET of all counters held high (counter resets when R is low) the count mode is enabled when CEP and PE goes high. When PE goes low the counters will synchronously load the data from the BFO inputs into the counters with the count occurring each 500 Hz. The counters output on TC only when PE is held high; however when CEP is held low the TC output will be retained until the next clock pulse. The TC output of the programmed dividers is connected to one input of a two input NOR gate U12A. The clock signal is connected to the second input so that any unwanted pulses, created by delay in the counters and not in sequence with the clock pulse will be rejected. The output of U12A is routed through inverter U12D to one clock input of the phase comparator as the oscillator reference frequency.

4. Reference Frequency. The 1 MHz reference frequency supplied from internal/external reference circuits is divided by 2000 to provide a 500 Hz reference frequency to the phase comparator. This division of 2000 is accomplished with two dual decade counters U8 and U9. Counter U8 provides a division by 100 while counter U9 provides division by 20. Each counter has two divide by 2 circuits and two divide by 5 circuits and are externally strapped to provide the divisions by 100 and 20. The division by 100 is accomplished by using all four dividers in the order shown (÷2 = 500 kHz. ÷5 = 100 kHz, ÷5 = 20 kHz and ÷2 = 10 kHz). The divide by 20 is accomplished in the same manner except its input is the 10 kHz output of the ÷100 and the second ÷5 is bypassed (÷2 = 5 kHz, ÷5 = 1 kHz, and ÷2 = 500 Hz). The resultant 500 Hz output is coupled to the clock input of D flip-flop U10A. This flip-flop is contained in a dual flip-flop package which together with NOR gate U11A make up the phase comparator.

5. Phase Comparator and Digital to Analog Converter. As described previously, the 500 Hz reference frequency is connected to flip-flop U10A. The second flip-flop U10B receives its clock signal from the programmed dividers. The D inputs of both flip-flops are tied to the +5 volts (logic 1) while both Q outputs are connected through 2 input AND gate U11A and resistor R83 to the reset of both flip-flops. Both flip-flops will reset each time that both Q's go high, causing a logic 0 at the resets of both flip-flops. The clock input signal to U10A (reference) consists of positive going pulses while the signal from the programmed divider (oscillator reference) also contains positive going pulses and is connected to the clock input of U10B. Each flip-flop triggers Q on (high) the positive going pulse of its respective clock signal and at the same time triggers $\overline{Q}$ to zero (low). Previously as described, when both Q outputs are high the output from AND gate U11A is low clearing both flip-flops through R83. This resets the Q outputs to low and the $\overline{Q}$ outputs to high. Refer to Figure 4-14. The two $\overline{Q}$ outputs are connected to the digital to analog converter which consists of transistors Q15, Q16 and Q17 and their associated components. This circuit operates in the same manner as the digital to analog converter

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described in Paragraph b (3) except that adjustments in the BFO frequency provide a different setting of the dc control voltage. This causes the VCO to change frequency in relation to the BFO setting.

6. Out of Lock Detector. The out of lock detector consists of NAND gate U11B, resistors R57, R58 and R84 and capacitors C83 and C86. This circuit operates in the same manner as the second local oscillator OOL circuit.

4.3.8 Receiver Control Section

The front panel Receiver control circuit card A9 provides for the in and out flow of Receiver control data, both from local (front panel) and remote locations. The front panel contains controls and indicators for local operation of the Receiver which includes: two - sixteen keypad switch sets, a tuning knob, two Liquid Crystal Displays (LCD), a fault indicator, an IF and AF GAIN control, two audio line level controls, an audio phones jack and a POWER-ON switch. All of these controls, except POWER-ON switch S1, are interfaced to Receiver circuits through the A9 circuit card. The IF and AF GAIN controls, two audio level controls and phones jack are routed directly through the A9 circuit card to their respective Receiver functions. The keypads, tuning encoder, LCD's and fault indicator connect through various interface circuits on the A9 circuit card to the microprocessor (A6A2). The data is processed by the microcomputer and routed back through interface circuits (A9) to various Receiver functions (A4, A5, A7 and A8). Receiver control data entered from a remote location is routed through interface circuits (A6A1) to the microprocessor (A6A2). This data is processed and routed through A9 in the same way as front panel data. Figure 4-16 shows a functional block diagram while the schematic diagram is shown on three sheets in Figure 7-11.

1. Front Panel Switches. Two sets of switch panels, each containing 16 pushbutton switches, are used to enter Receiver control data from the front panel. Switch panel 1 is used for Receiver tuning, BFO tuning and for selecting remote or local control. Switch panel 2 is used to select Receiver mode, AGC mode, bandwidth and RF/AF meter indication. Each pushbutton switch is a single pole, single throw switch with normally open momentary contacts. One contact of each switch is commonly connected to ground within each keypad set. The other contact of each switch is connected to an input of six hex buffers U7, U8, U9, U23, U24 and U25 (two inputs of U8 and U24 are unused) and to +5 volts through a 10K ohm resistor supplied through resistor array U1, U2, U5 and U6. When any particular switch is open (not pushed), its input to the buffer is held high through the 10K ohm resistor to the +5 volts. When the switch is closed (pushed), the input line to the buffer goes low. The high or low condition of any switch is passed through the respective buffers to the data bus when that particular buffer is enabled from the address multiplexer U29. The 32 outputs (four are unused) of the six hex buffers are strapped to the 8-line data bus in groups of eight with each group controlled from a separate address enable signal from U29. This assures that the status of two or more switches will not be transferred through the buffers to the same data line at the same time. The enable signals from U29 are controlled from in/out read and address control signals generated by the microprocessor in order to regularly scan the switch pads for new data. Data on these lines are transferred to the microprocessor as described in 5.

2. Tuning Encoder. The tuning encoder, operated from the front panel tuning knob, is used to adjust, in fine frequency increments, either Receiver frequency or BFO frequency. Pushbuttons, on the right keypad, select the mode of the tuning encoder and the rate at which frequency data may be entered. The TUNE RATE pushbutton selects one of three rates of change for main Receiver frequency that the tuning encoder will respond; fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments). The BFO pushbutton selects BFO frequency tuning in one rate only (10 Hz increments). The LOCK pushbutton disables the encoder while the TUNE RATE or BFO pushbutton enables the encoder from a locked condition. The tuning encoder consists of a 25 segmented disk operating in conjunction with two offset reflective object sensors U59 and U60 with the sensors being mounted on the A9 circuit card. The light from the sensor is reflected from the alternately reflective and non-reflective segments of the disk to the detectors as the disk is rotated.

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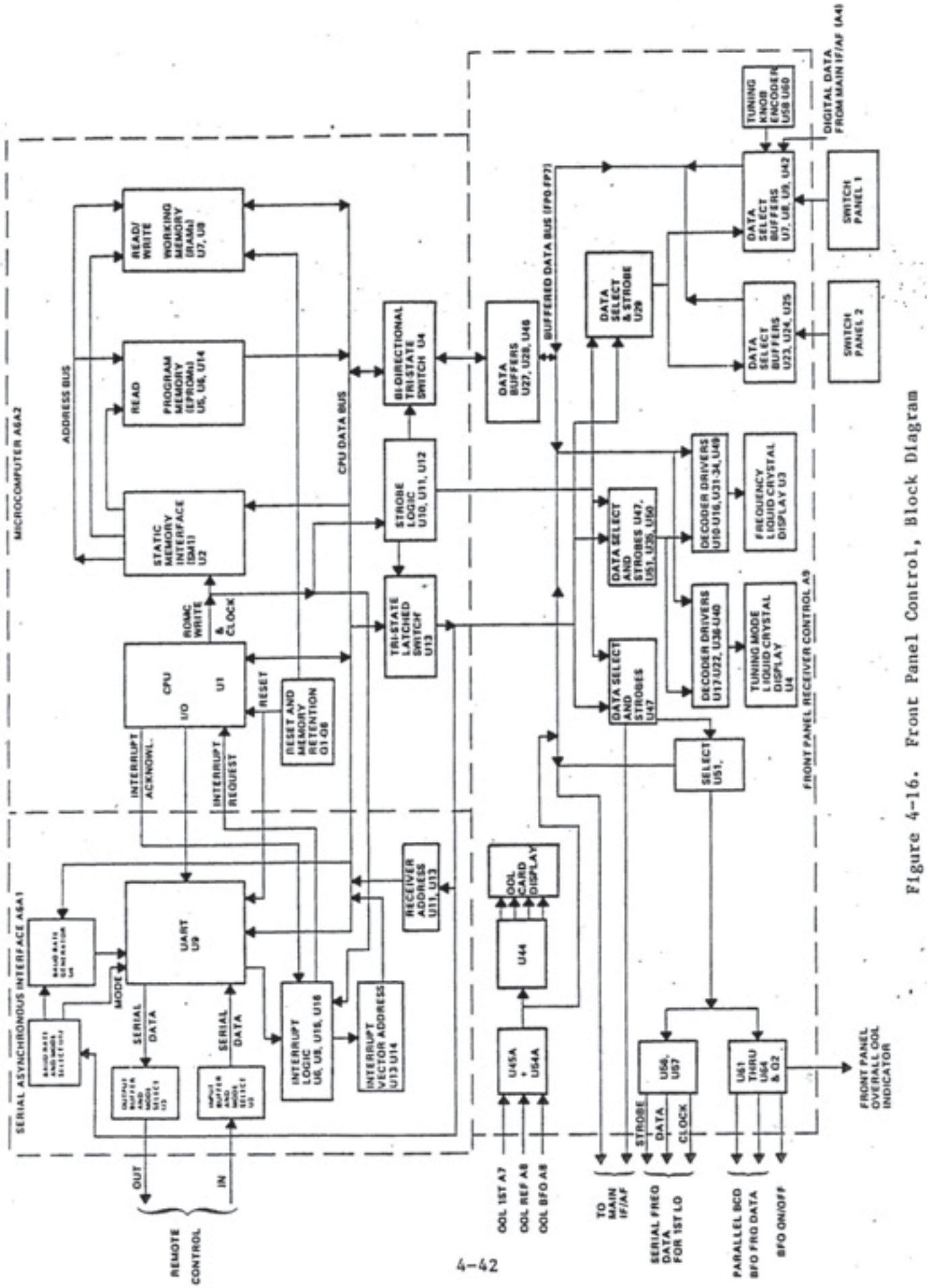

Figure 4-16. Front Panel Control, Block Diagram

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This produces two pulse waveforms (see Figure 4-17). The two detectors are physically positioned, in relation to the disk segments, so that one waveform either leads or lags the other by 90 degrees. Clockwise rotation of the tuning knob causes the output of U59 to lead that of U60 causing frequency entered to increase. Counter-clockwise rotation causes the waveform of U60 to lead that of U59 causing frequency to decrease. The outputs of the object sensors are coupled, through resistors R16 and R17, to a comparator U58A and U58B. The two inputs to this circuit are compared to a fixed dc voltage input to the comparator from resistor combinations (R8 and R10 for U58A and R9 and R11 for U58B) which control the comparator switching point. The square wave outputs of the comparator are routed to buffer U42B. This data buffer is enabled, from multiplexer U29, in program sequence to transfer the encoder data to data lines FP0 and FP1 for processing as described in item 5.

3. Audio and IF. Audio and IF controls and an audio phones jack are contained on the front panel for control and monitoring of these functions. Control and audio to and from these components are routed through the A9 circuit card from the A4 circuit card with no connection to the in-out digital control hardware on A9. A complete description of their function can be found in Paragraph 4.3.4.

4. Liquid Crystal Displays. Two Liquid Crystal Displays (LCD) are contained on the front panel for displaying Receiver status. Receiver frequency and BFO frequency are displayed on LCD U3 while Receiver mode, AGC mode, tuning mode, remote/local mode, bandwidth and AF/RF metering are displayed on LCD U4. The 8-line data bus is routed directly to ten 4-line LCD drivers (U19-U22, U36-U40 and U49) and to thirteen BCD to seven segment decoder/drivers (U10-U18 and U31-U34). The ten line drivers provide decoding and drive for all annunciator displays while the thirteen 7-segment drivers provide decoding and drive for all numerical displays. Multivibrator U26, timed by R1 and C8, provides a 100 Hz signal to the DF (display frequency) inputs of the line drivers, the BP (backplane) inputs of the 7-segment drivers and the two LCD's. This signal is used to drive the LCD's display.

NOTE

LCD displays operate from low frequency square wave pulse trains. The contrast of the display being a function of the frequency.

Timing to the line drivers is provided by strobe signals from BCD to decimal decoder U50 while the 7-segment drivers receive timing from 4-bit latch and decoder U35. These two decoders receive their input from binary counter U51. The clock pulse (CP) for U51 is derived from three strobes S7, S11 and S15 combined by NOR gate U48A. Decoder U35 is controlled by inversion of strobe S7 through U48B while U50 is timed by strobe S15 through inverter U56. When a strobe signal in program time enables a line driver or 7-segment driver, the data at its input port is latched into the driver. The 100 Hz signal on the DF or BP input of the drivers is applied to the display segments and is inverted or not inverted through control of the data input to each driver. This in turn controls whether the segment is turned on or off. Any segment of an LCD is turned on by a 180 degree difference of phase between segment input and the main backplane drive to the LCD (Figure 4-18). To turn the display segment off the phase difference between these two signals must be zero degrees; that is, the two signals must be in phase (see Figure 4-18).

5. Receiver Control Circuit Card A9. This circuitry routes data entered at the front panel, to the microprocessor bus and routes processed data from A6A2 to various receiver functions on A4, A5, A7 and A8 circuit cards. This data flow in the data bus I0D0 through I0D7 is controlled by read, write and address controls (I0C0 through I0C7) signals from the microprocessor. All data entered from the front panel except audio and IF functions described in item 3, is transferred to the

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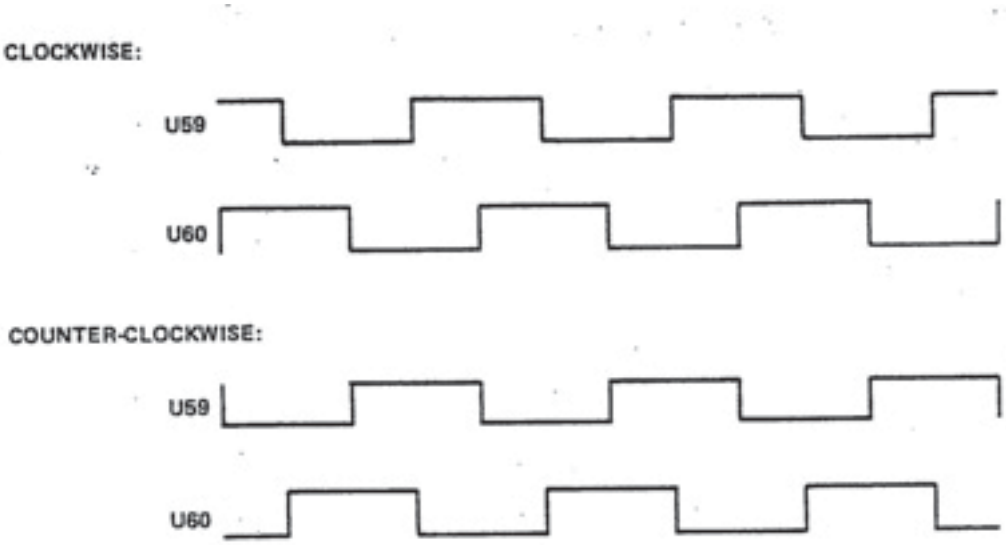

Figure 4-17. Encoder Output Signals

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microprocessor for processing, then routed back through A9 to various Receiver functions. Data entered from a remote location is routed to the microprocessor, then the processed data is routed to various Receiver functions through A9 in the same manner as processed front panel data.

a. Data In/Out Control. Data flow between the A9 circuit card and the microprocessor is via their respective 8 bi-directional data lines. The flow of data from A9 to A6A2 and vice versa is buffered and controlled by U27, U28 and U46. The bi-directional switches U27 and U28 are configured to transfer data from A9 to A6A2 when enabled in a READ cycle via inverter U56. The tri-state, 8-bit latch U46 is used to transfer data from A6A2 to A9 during a WRITE cycle under the control of the WSTB signal. Control signals (I0C0 through I0C3) from the microprocessor are used to generate strobe signals are timed through the WSTB signal to the strobe input of U47 and from multivibrator U55A and U55B. The multivibrator, controlled from the WSTB signal and inverted I0C5 signal through NOR gate U48, provides timing to the inhibit input of U47. The strobe signals (U47 outputs) are then latched in proper timed sequence and are used to time latches, decoders, gates, etc., that in turn control data flow to various receiver control functions or displays. The data flow through these components and the strobe signal functions are described in the various receiver functions that follow.

b. Receiver Frequency. Processed receiver frequency data from the microprocessor is routed through data line FPO to one input of two input AND gate U57A. The second input to the AND gate comes from the Q0 output of decoder U64 which receives its input from presettable binary counter U51. Strobes S5 and S7, S11 and S15 through NOR gate U48 time U51, strobe S11 through inverter U56 time U64. The frequency data in proper timed sequence is serially routed through AND gate U57A to the A7 circuit card. Strobe signal S12 and the Q0 output of U64 are connected to two input AND gate U57B whose output is routed to A7 as a clock signal for circuits on that card. The Q0 output of U64 is also routed to A7 through inverter U56 as a strobe signal to those same circuits. These circuits on the A7 circuit card further process the serial frequency data in conjunction with the clock and strobe signals, and adjust the oscillator frequency as first directed from the front panel or remote location.

c. BFO Frequency. BFO frequency data after being processed by the microprocessor (A6A2) is routed through data lines FP0, FP1 and FP3 to the same binary counter (U51) as the Receiver frequency data. Outputs (Q1, Q2 and Q3) of the binary counter are connected to the three binary inputs of four 8-bit addressable latches U61 through U64. These latches supply the BCD inputs to a programmed divider circuit on the A8 circuit card for BFO frequency control. Timing for the latches is supplied by strobe S11 through inverter U56. The Q4 output of latch U61 provides a signal through transistor Q2 that enables the BFO synthesizer on A8 in CW and SSB/ISB modes.

d. Circuit Card A4 Functions. All eight data lines along with six strobe signals are routed to control circuits on the A4 circuit card for control of various receiver functions operating on this circuit card. The control circuits (located on A4) are a direct function of the A9 interface circuits; therefore, a description of their operation is included in this paragraph. All references to components in this paragraph (unless otherwise noted) refer to components on the A4 circuit card. Refer to Figure 7-4 for the schematic diagram. The eight data lines of A9 are routed to 2-level translators (U3 and U5) on the A4 circuit card. Six strobe signals (STB10 through STB15) are also routed to A4 with strobes STB12 through STB15 connected to the input of level translator U16. These level translators provide a new voltage level to the incoming data for operation of circuits on the A4 card. The strobe outputs from translator U16 are used to clock data latches U2, U4, U13, U15 and U23, the digital-to-analog converter U21, and the crosspoint switch U25. The data bus output from translators U3 and U5 is routed to these components and applied to the various A4 functions as directed by the strobe signals. Data latch U2 is used to select the bandpass filters, but through

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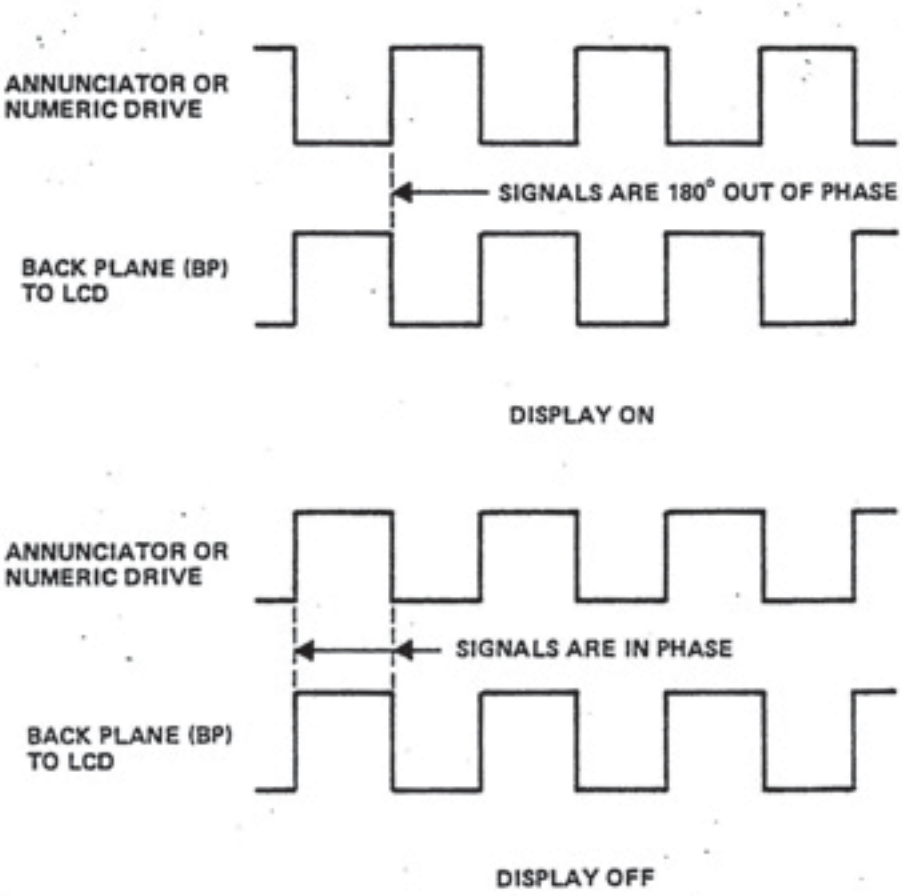

Figure 4-18. Liquid Crystal Display Control Signals.

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BCD to 1 of 10 decoder U1. This decoder has only one output high at a time as directed by the BCD input. This allows selection of filter slots FL2 through FL7 in accordance with the three digit BCD on the data line as clocked by strobe 12 on the clock input of U2. The Q4 output of U2 is routed directly to the diode switch of FL1 which is used to select that filter slot at the appropriate program time. Data through data latch U4 is used to control the RF switch that selects between BFO and the IF signal for input to the limiting amplifier and FM detector and D flip-flop U9A. This flip-flop controls the AGC dump line. Data latch U4 is also timed by strobe 12. Data through data latches U13 and U15 control switches in the AGC circuits for various AGC modes. These latches are timed through strobe 13. The output of data latch U23, timed by strobe 15, controls the detector select switch U19A, an audio filter level control switch U19B and an AF meter audio select switch U19C. All eight data lines are connected to the digital-to-analog converter for digital control of its analog output. This unit is timed through strobe 14 and is used to provide analog-to-digital conversion of the DIV AGC line and audio line by peak detector U22A using a successive approximation technique. The digital information gathered by the microprocessor is used for front panel metering. Five data lines are routed to crosspoint switch U25 which is timed by strobe S15. The audio function of the crosspoint switch along with other A4 functions controlled through A9 are described under the A4 circuit card in Paragraph 4.3.4.

e. Circuit Card A5 Functions. Two data latches on the A5 circuit card are used to control AGC circuit functions on this circuit card. The two latches U7 and U8 have A5 reference designators and are shown on the A5 schematic diagram in Figure 7-5. The 8-line data bus from translators (described in Paragraph d) on the A4 circuit card are routed to the data latches with strobe 10 timing both latches through transistor Q6, also located on A5. The data output from the latches is used to control the AGC circuits described under the A5 circuit card in Paragraph 4.3.5.

f. Out of Lock (OOL) Functions. Three out of lock circuits, that monitor the condition of the phase lock loops of the three oscillators, drive OOL indicators on the A9 circuit card and supply their output data to the microprocessor. This data is routed through circuits on the A9 card that drive a fault indicator on the front panel and also a fault indicating circuit that provides a TTL level related to the FAULT condition to connector J3 on the rear panel via A4 circuit card. The three OOL circuit outputs from the three oscillator phase lock loops are connected to the S inputs of dual D flip-flops U45 and U54. These flip-flops are clocked from address multiplexer U29. With the data and reset inputs tied to ground (low) and the S inputs low (phase lock loop in lock) the Q outputs of the flip-flops will be low. If an S input goes high (out of lock) its Q output will go high causing a low through its respective inverter U44A, U44B or U53A. This in turn will enable the applicable LED indicator DS1, DS2 or DS3. These LED indicators are located on the A9 circuit card for accurate determination of the OOL circuit. The Q outputs of the flip-flops are also connected to the inputs of buffer U43 which is also timed by multiplexer U29. The buffer, in program sequence, outputs the status of the OOL circuits on the data bus which is then routed to the microprocessor. The processed FAULT data is routed through binary counter U51 and decoders U63 and U64. The Q5 (FAULT) output of decoder U63 is routed through inverter U52B to the rear panel while the Q5 (FAULT) output of U64 drives the front panel fault indicator through inverter U52A.

g. AF/RF Meter Comparator Functions. The main RF, ISB RF, and AF comparator circuits along with an ISB fitted circuit from the A4 circuit card are connected to four inputs of non-inverting buffer U42A. The inputs are strapped to +5 volts through 22K ohm resistors in resistor array U41. When the optional A5 circuit card is installed, input I1 is strapped low through a grounding circuit on that card. The three comparator input (I2, I3 and I4) levels depend on the comparator outputs. Buffer U42 is timed from multiplexer U29 and in program sequence transfers the comparator data as used by A6A2 in a successive approximation technique to generate a bar graph for front panel display to data lines FP0, FP1 and FP2 and the ISB fitted status to data line FP4.

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h. Power Supply Distribution. The A9 circuit card provides a distribution path for dc power, generated from the A10 power supply module directly to circuit cards A4, A6A2, A7 and A8. This dc power through A9 is further distributed through the A4 circuit card to the optional A5 circuit card and through A6A2 circuit card to optional A6A1 circuit card. The +15 volts dc is also routed to the front panel for operation of the LCD back lighting. The distribution of this dc power is as shown below.

	From A10	Output To			
DC Power	To A9J4 Pin Number	A4 from A9J5 Pin Numbers	A6A2 from A9W1 Pin Numbers	A7 from A9J6 Pin Numbers	A8 from A9J7 Pin Numbers
+5 Volts	3, 4, 7 and 8	1	23 and 24	20	26
+5 Volts (unregulated)	9 and 10		15 and 16	15 and 16	
+5 Volts	13, 15, 19, 21 and 22	2 and 4	19 and 20	17 and 18	24
+ 15 Volts (unregulated)	5 and 6	8			
−15 Volts	18 and 20	6	21 and 22	14	22
+20 Volts	1 and 2				

4.3.8.1 Microcomputer Board A6A2

A functional description of the microcomputer board A6A2 is given in Paragraph 4.2.4 with a functional block diagram shown in Figure 4- 20.

As shown on the electrical schematic diagram, Figure 7-8, the microcomputer board A6A2 makes use of a type 3850 CPU (U1). The 3850 CPU is from the Fairchild F8 microcomputer component family. A detailed description of the microcomputer family operation, including timing and instruction set, is given in the F8 Users Guide. This guide is available from the Fairchild Camera and Instrument Corporation, Mountain View, California.

The CPU (U1) controls receiver operation by reading the operating program and routing data and control signals throughout the receiver based on the procedures and algorithms of this program. The CPU 8-bit data word bi-directional ports (DB0-DB7) connect to an 8-line data bus. This bus is common to major receiver control circuitry (directly or through buffers) and is the primary means of communication between the CPU and other parts of the receiver. The CPU clock is provided by the 2.0 MHz crystal Y1 which is connected across pins 38 and 39 of the CPU. The Φ and Write pulse outputs (shown in Figure 4-19) are clock outputs which provide timing drive for all microcomputer circuitry. The ROMC-0-4 outputs from the CPU connect to other circuits in the receiver and identify operations which these circuits must perform during any instruction cycle. Interrupt requests are received through the /INT REQ port while the acknowledgement that the CPU will respond to the interrupt requests is routed through the /ICB port. The Input/Output (I/O) ports 00-07 and 10-17 are ports through which the CPU communicates with logic external to the microprocessor. Here, seven of these ports are used and are connected to the serial asynchronous interface module A6A1 (when it is installed in the receiver).

Figure 4-20 is a functional block diagram of the CPU. The inputs and outputs, described previously, are shown as well as the basic functions performed by the CPU. The CPU performs

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instructions which are obtained from the control program contained in the program memory (EPROMs, U5, U6 and U14). These instructions are routed to the instruction register of the CPU and then carried out during instruction cycles. The control unit logic of the CPU sends out the ROMC signals to other parts of the Receiver during each instruction cycle. These specify the functions to be performed for each instruction. There are four or six clock periods (Figure 4-19) in an instruction cycle (dependent upon the number of 8-bit instruction words required), which are determined by the ROMC signals generated by the CPU. The CPU performs computations, when required by the program, in its ALU (Arithmetic Logic Unit) making use of the accumulator, status register and scratch pad memory registers. The ISAR (Information Storage Address Register) is the address register for the scratch pad memory.

The CPU receives and follows the program (sequence of instructions) which is stored in the erasable/programmable read only memory (EPROMs) contained in U5, U6 and U14 (Figure 7-8). These are type 2716 EPROMs. Each of these units contains 2K 8-bit words for a total of 6K 8-bit words of programmable memory. The CPU also uses the temporary Random Access Memory (RAMs) contained in U7 and U8. These are type 5101L RAMs and provide 256 8-bit words of working memory (temporary data storage). U7 provides 4 bits of each 8-bit word and U8 provides the remaining 4 bits of each word.

The memories are addressed by the CPU through U2, the Static Memory Interface (SMI) type 3853 (Figure 7-8). The CPU sends the ROMC-0-4, Write and Φ signals to the SMI. The SMI, in timed sequence, recognizes the ROMC-0-4 code for a memory access operation, and addresses the appropriate memory, program (EPROM) or working (RAM), over the address bus A0-A10. The SMI (U2) address outputs A11 and A12, through decoders U3A and U3B are also used in addressing by enabling the appropriate memory chip U5-U8 and U14. Directed by the ROMC-0-4 code and write signals from the CPU, the SMI also directs reading or writing through its CPU READ and /MEM W outputs. Thus, the memory units (when addressed and directed place data on the CPU data bus or accept data from the CPU data bus (DB0-DB7). The EPROMs place 8-bit instruction words on the bus and the RAMs supply data to or read data from the bus when addressed and directed by the CPU under program control.

Figure 4-21 is a functional block diagram of the System Memory Interface (SMI). The inputs and outputs, described previously, are shown. The SMI contains the program counter which contains the program memory address (at which instructions are located) and the data counters which contain the working memory (RAM) addresses. The program counter is either incremented as each instruction in the program is executed or new addresses are inserted by the program or by the interrupt address vector. The working memory addresses are generated by the program. The SMI also contains a timer which is used to generate internal interrupts for initiating program subroutines at required times during the program cycle.

As described previously, the CPU (under program control) writes and reads data to and from the front panel controls and displays and the receiver circuitry. This data consists of front panel control settings, display readouts and receiver circuit control and status signals in the form of 8-bit digital words. The CPU data bus (D00-D07) connects to these units via the tri-state bi-directional switch U4 (Figure 7-8) and then through the bi-directional data bus (I0D0-I0D7). The direction of data flow and timing of switch openings are controlled through pins 1 and 19 of U4. Signals to these pins are generated by the strobe logic gates U10-U12 and the Q7 output from the tri-state latched switch U13 at the appropriate times in the program. The strobe logic inputs consist of the ROMC-0-4 and write signals. Thus, at appropriate program times, the CPU data bus connects through U4 and through pins 1-8 of connector J2 to the front panel and receiver control circuitry. Also, outputs /IO READ and /WSTB from pins 25 and 27 of J1 go to the front panel and receiver control circuitry to direct reading or writing data from or to the bus at the appropriate times in the program. The U13 latched outputs (I0C0-E0C7) provide the programmed codes

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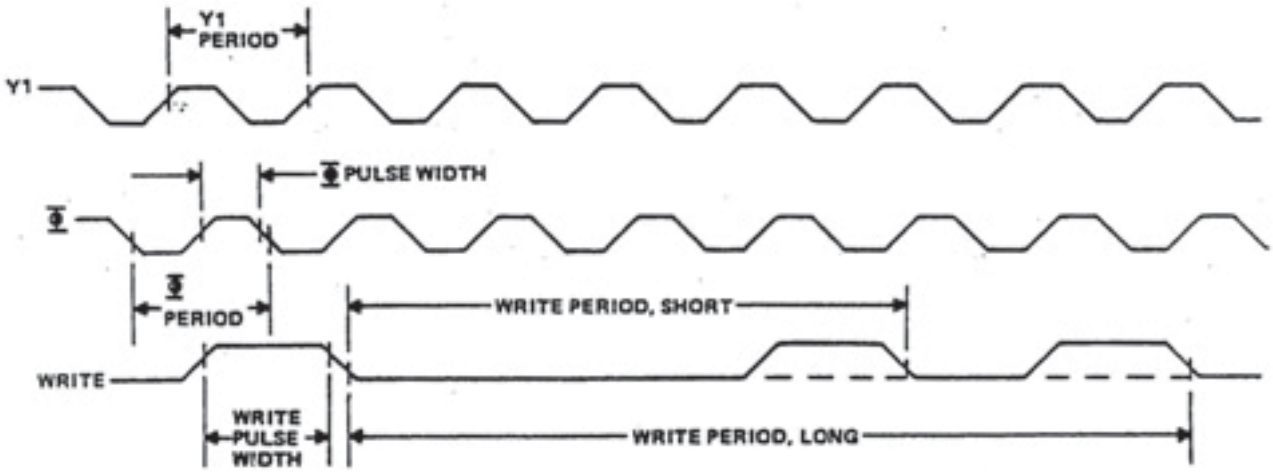

Figure 4-19. Central Processor Unit Timing Signal Diagram

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for the selection (or addressing) of the various elements in the front panel and receiver control circuitry (to accept or supply data from or to the common data bus) at appropriate times in the program. These addresses (I0C0-E0C7) are latched into the U13 outputs from the CPU data bus (D00-D07) at the proper times in the program through the U13 OE (output enable) and CP clock inputs. The OE and CP inputs are generated by the ROMC-0-4 and write outputs from the CPU through gates U10 and U12. The CPU also receives and sends data from and to the Serial Asynchronous Interface modules (A6A1) via the data bus. This data consists of commands and receiver settings to the CPU and receiver status to the remote controller in the form of 8-bit digital words. Connections between these units are made through connector J2. The data bus to the Serial Asynchronous Interface module is labeled PB0-PB7. The microcomputer receives the interrupt request (/INT REQ) signal from the Serial Asynchronous Interface module. The CPU also sends the WRITE, Φ timing signal, strobe logic outputs /IO READ and /WSTB, the tri-state latched outputs I0C0-I0C7, the ROMC-0-4 outputs, the CPU 00-07 and 10-17 outputs and the interrupt acknowledge /ICB signal. These signals are used to direct operations of the interface module and to synchronize operations between the CPU and the remote controller, as will be described later.

The reset and memory retention system is composed of stages Q1 through Q7, the 2.0 volt internal power source BT1, R9, CR3 and C16, and the battery charging circuitry, CR6, R9. At Power On, the +5 Volt unregulated line (from pins 15 and 16 of J1) switches Q1 and Q2, bringing the /RESET line high. Also at Power On/RESET turns Q4 and Q5 on, C15 is charged, the gate of Q6 is taken negative and CE2 of the RAMs (U7 and U8) is asserted. This activates the RAMs in their normal operating, higher power drain, mode. Also, the gate of Q7 goes negative taking the low off the CPU RESET. The CPU now starts the initialization process. During the turn on cycle the +12V through R8 quickly turns on Q3, charging C16, which supplies Vcc to the RAMs. CR2 limits the voltage to Vcc while R11 limits the current. CR3 is back biased and the +5 volt supply through CR6 and R9 charges the internal battery BT1.

The Schmidt trigger, Q1 and Q2, detects voltage variations in the +5 volt unregulated line. The collector of Q2 will go to ground when the power supply +5 volt unregulated line decreases (such as at power turn off or failure) past the trigger levels set by CR1 and R2-R5-R6. When this occurs, the /RESET line goes low. Also, the voltage at D of Q7 going low, instructs the CPU to come to a stop at the end of the next execution cycle. At power down, Q3 will stop conducting. Initially, the voltage across C16 still supplies sufficient VDD voltage to the RAMs for the CPU to complete its cycle. When the voltage across C16 falls to approximately 2.4 volts the internal battery BT1, through R9 and CR3 supplies the memory retention power to the RAMs. The voltage out at D of Q6, now low, sets the RAMs at their lower power drain memory retention mode. The battery leakage is greater than the retention memory current drawn by the RAMs; therefore, several months of memory retention is available.

The CPU may receive an interrupt request (/INT REQ) into its pin 23 from the SMI (internal interrupt) or from the Remote Controller Serial Asynchronous Interface (when used) through J2. During an interrupt routine, the CPU will assert its /ICB output (from pin 22), thus not accepting any further interrupts until it has completed the routine. When a Remote Controller Serial Asynchronous Interface is not used, with no J2 connection and with LINK 1 installed (see Figure 7-8),the /ICB output from the CPU connects directly to the /PRI IN input of the SMI. This prevents an internal interrupt from being generated by the SMI until any previously accepted interrupt has been serviced by the CPU. When a Remote Controller Serial Asynchronous Interface is used with the interface connected to J2 and LINK 1 removed, the /ICB output goes directly to the Serial Asynchronous Interface circuitry. As will be described in more detail later, this prevents the interface from generating an external interrupt until any previously accepted interrupt has been serviced by the CPU. In addition, the PRI input (into pin 24 of J2) from the Serial Asynchronous Interface goes to the /PRI IN of the SMI. The Serial Asynchronous Interface is waiting to request an interrupt. Thus, the SMI cannot generate an

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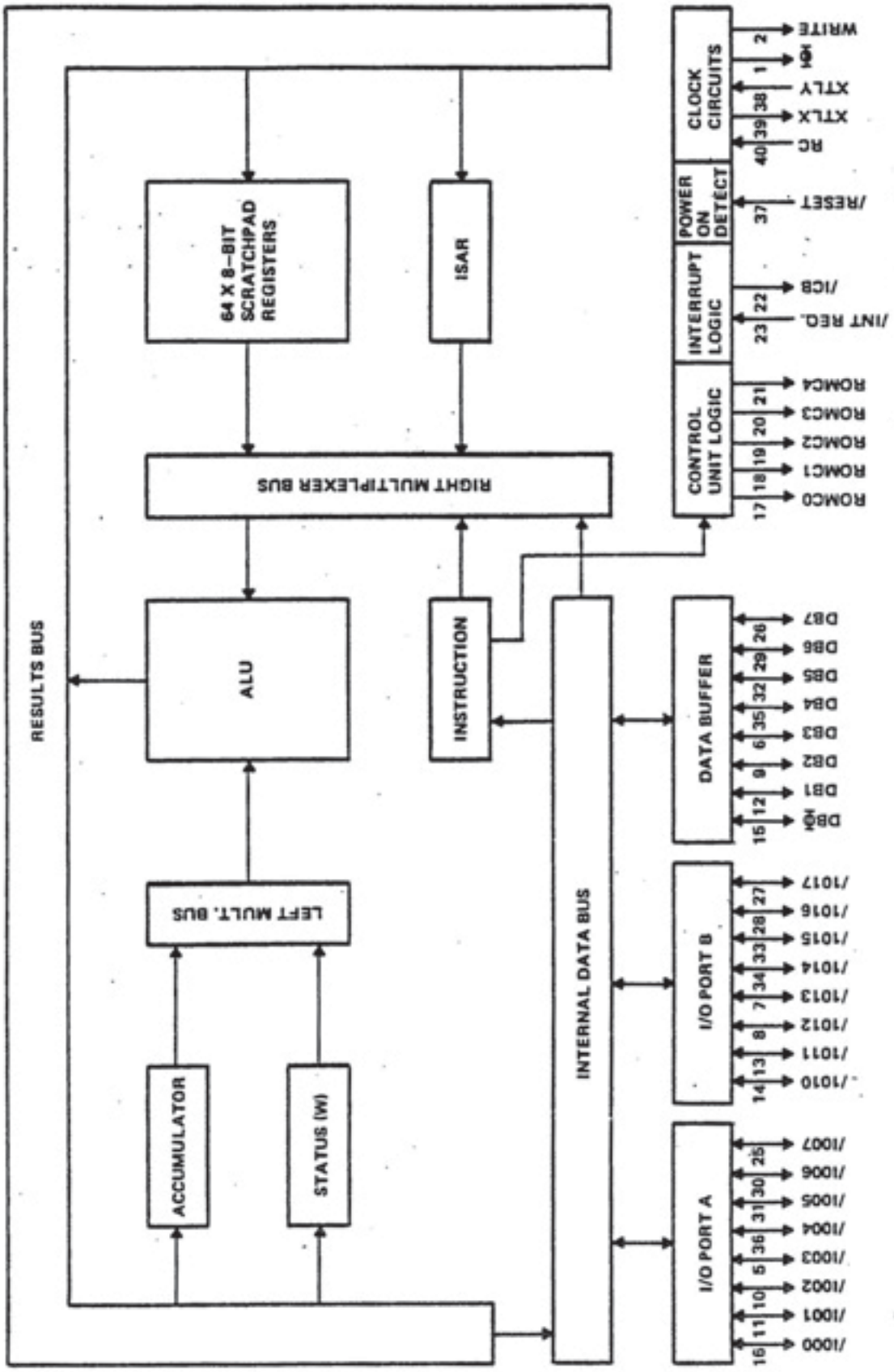

Figure 4-20. Central Processor Unit Functional Block Diagram

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internal interrupt while either of these conditions exist. It will be noted that the DR and TBRE outputs from the UART (in the Serial Asynchronous Interface, see Figure 7-7) are sent out through connector P1, pins 37 and 36, to the CPU I/O terminals 11 and 10. These are used by the microcomputer to determine whether the interrupt request was for a receive or transmit routine.

The error outputs from the UART; PE (parity error), OE (overload error) and FE (framing error) are sent to the CPU I/O ports 14, 13 and 12 through connectors P1 pins 5, 43 and 42.

4.3.8.2 Serial Asynchronous Interface Module A6A1

A functional description of the Serial Asynchronous Interface Module is given in Paragraph 4.2.4 in conjunction with the functional block diagrams, Figure 4-16 and 4-21.

Figure 7-7 is the electrical schematic diagram of the Serial Asynchronous Interface Module A6A1. This module interfaces an external remote controller (when used) through a serial data line to the microcomputer through an 8-bit data bus. The Universal Asynchronous Receiver transmitter, UART (U9), provides the interface between the serial data lines to and from the remote controller and the microcomputer parallel data bus (PB0-PB7).

The UART contains a transmit and a receive station. A block diagram for each of these sections is shown in Figures 4-22 and 4-23. The receive section converts the incoming serial stream (from the remote controller into the pin 20 RR1 input) to 8-bit parallel words and places them on the microcomputer bus through output pins 5 through 12. The transmit section, when directed by the microcomputer (through pin 23, data strobe TBRL) takes the 8-bit parallel words from the microcomputer data bus (through pins 26-33) and puts them in a serial format for serial transmission to the remote controller (through pin 25). The serial format,Section III, Paragraph 3.3.3.2, is an 11-bit word containing one start bit, the 7-bit ASCII Code data word, a parity bit followed by two stop bits. Coding for the data word is described in Section III, Paragraph 3.3.3.2. The UART parallel inputs and outputs are tied together and onto the common microcomputer data bus (Figure 7-7). The UART receiver inputs and outputs are tri-state, with only inputs or outputs activated at one time.

The UART is initialized by the /RESET line from the microcomputer, through pin 2 of connected P1 and inverter U6A, into its MR (pin 21) input. Transmit and receive clock signals, TRC and RRC (pins 40 and 17), which determine the rate of data transfer, are supplied by the programmable Baud Rate generator U4. This generator divides the frequency of crystal, Y1, down to the programmed transmit and receive clock rates. Both the receive and transmit clock rates are set at 16 times the baud rate. The frequency generated by U4 is obtained from the data bus, upon initialization by the microcomputer program from information supplied by the configuration set on the rear panel cover into its input RA-RD and TA-TD. This data is strobed into U4 by the strobing signal from output VO (pin 14) of decoder U19. This decoder is driven by microcomputer address and strobing signals I0C0-I0C1, I0 READ and /WSTB. As indicated by Table III on the A6A1 schematic diagram, the baud rate is set by connecting the appropriate A6A1W1J1 external connector terminals W, X, Y and Z to common. Terminals not connected to common will have +5V connected through U1. These terminals connect to inputs of tri-state buffer U12. The inputs are strobed onto the data bus (to go to the baud generator inputs, at the appropriate times), by the strobe signal out of X1 (pin 4) of decoder U19. The baud rate is set to match that of the Remote controller. Table 2-7 gives information for setting the baud rate.

Also strobed, upon initialization, from output Y1 of decoder U19 is the CRL (pin 34) input to the UART. This loads the UART control register with the EPE, CLS1, CLS2, SBS and P1 inputs at that time. This sets whether parity is used (P1) odd or even parity (EPE), number of bits in a data word (CL1, CL2) and number of stop bits (SBS) used. As described previously, the

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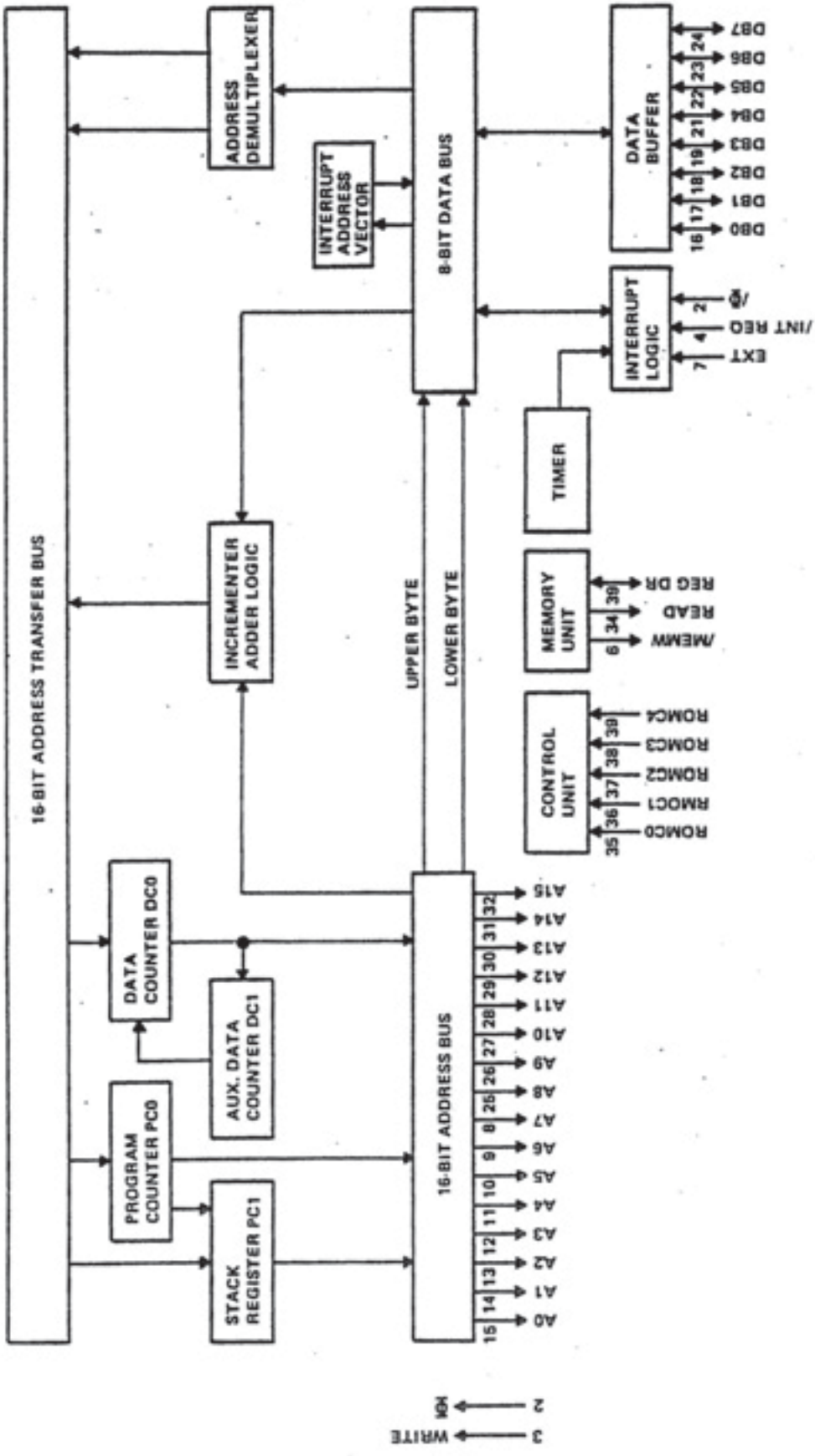

Figure 4.21. System Memory Interface Functional Block Diagram

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word length is fixed at 8 and the number of stop bits is fixed at 2. Table I on the schematic shows that the parity (ON or OFF) and even or odd parity are set through terminals U and V of external connector A6A1W1J1. These are also set by connecting the appropriate terminals to common ground. The unconnected terminals will have +5V connected through U1. These terminals also connect to tri-state buffer U12 and are strobed on to the data bus (and to P1 and EPE) at the appropriate time by the strobe signal out of X2 (pin 4) of decoder U19.

The receiver number for remote addressing is selected by connecting the appropriate terminals K, L, M, N, P, R, S, T of connector A6A1W1J1 (See Table I on schematic) to common. This setting through tri-state buffers U11 and U13B and Pull-up resistors U10 and U1 is strobed onto the data bus, for readout by the microprocessor, by the strobe from X1 (pin 3) of decoder U19.

Figure 4-23 is a block diagram of the receive station of the UART. When data is received from the remote controller, it comes through the external connector A6A1W1J1 to Receiver U2. Receiver U2 yields signals that are compatible to the Receiver circuits of the UART (U9) through its RR1 input (pin 20). The UART receiver section converts the incoming serial data stream from the remote controller to 8-bit parallel words and places them on the microcomputer bus (PB0 through PB7) through outputs RBR1 through RBR8. The serial format, as described previously, is an 11-bit word containing a start bit, a 7-bit ASCII code, a parity bit followed by two stop bits. Instruction word codes are also described in Section III. When data is available from the remote controller, an interrupt request is made by asserting the DR output, indicating data is available to the microcomputer. The DR output will go through gate U8A, if not inhibited by computer outputs 00 and 01 (microcomputer not accepting these interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D, and U17B) to drive flip-flop U16A. The outputs of this flip-flop drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. If the CPU is currently blocking, thus ignoring interrupt requests, /ICB will be high. Under this condition U15B and C gates are inhibited. When /ICB is not high (microcomputer accepting interrupts), gates U15B and C are enabled. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its normal Receiver monitoring functions as directed by the control program (from EPROM) and start the interrupt routine to accept data from the remote controller.

During the interrupt routine the microcomputer asserts its /ICB output, thus not accepting any further interrupts until it has completed the routine. It will be noted that the DR output from the UART are routed through connector P1, pin 37 to the microprocessor I/O terminal 11. This input enables the microcomputer to determine that the interrupt request was for a receive routine.

Figure 4-22 is a block diagram of the transmit section of the UART. When the remote controller has requested data (status) and the transmit buffers of the UART are empty, so that it can accept data from the microcomputer for transmission to the remote controller, the TBRE output is asserted. The TBRE signal will go through gate U8A, if it is not inhibited by microcomputer outputs 00 and 01 (microcomputer not accepting interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D and U17B) to drive flip-flop U16A. The outputs of these flip-flops drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. When the CPU in the microcomputer is busy and ignoring interrupt requests, /ICB will be high. Under this condition, U15B and C gates are inhibited. When /ICB is not high these gates (U15B and C) are enabled and the /PRI output from U15C is output through pin 24 of P1. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its present program and start the interrupt routine to send

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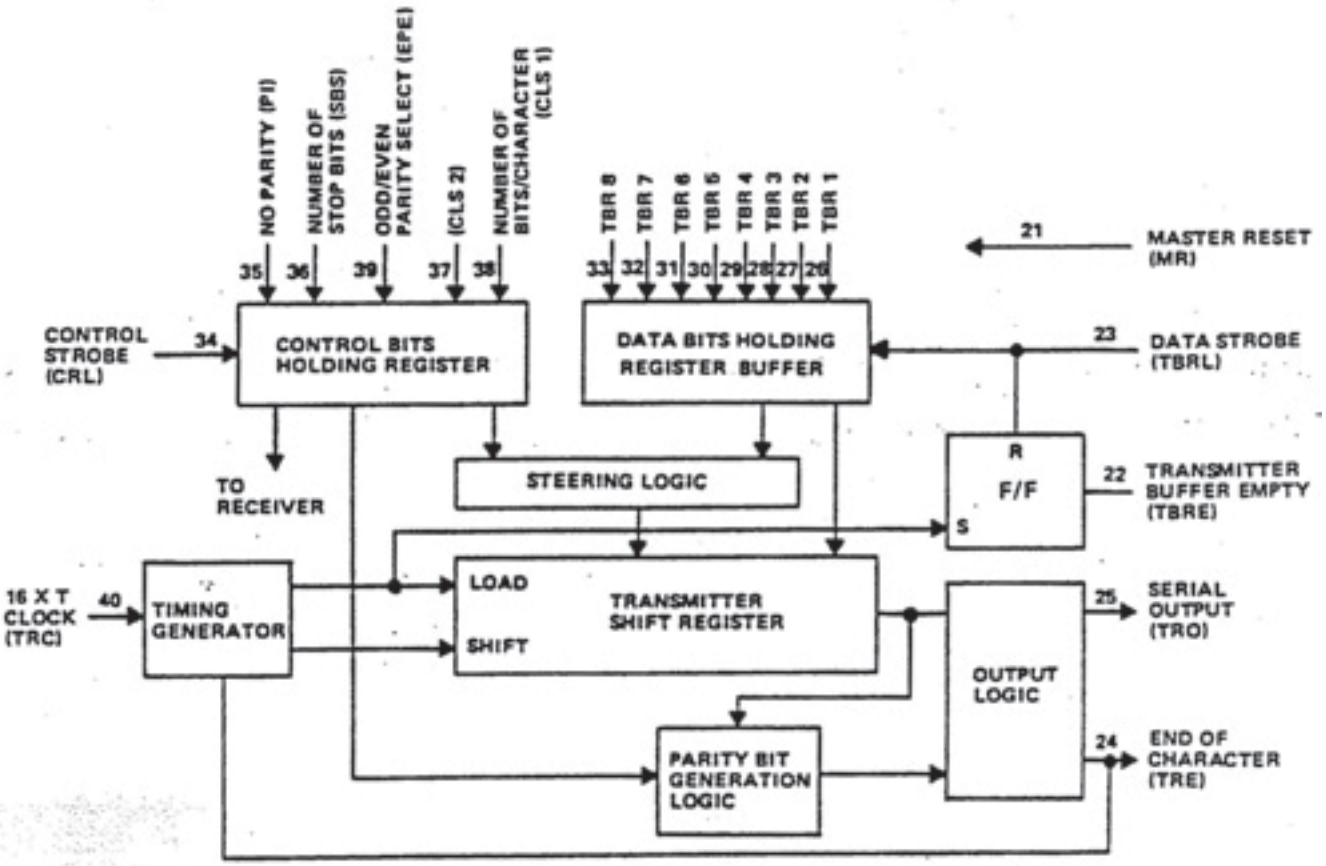

Figure 4-22. UART Transmitter Functional Block Diagram

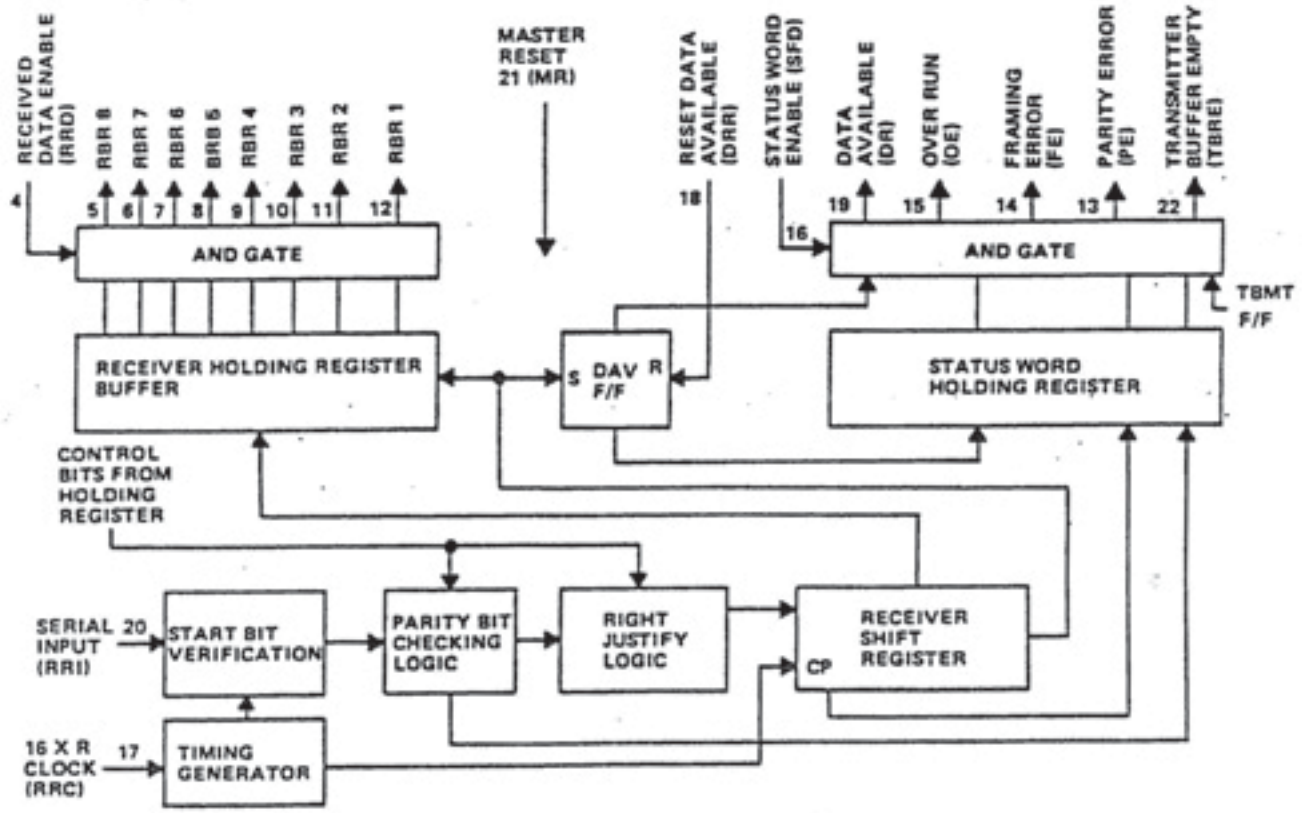

Figure 4-23. UART Receiver Functional Block Diagram

receiver status to the remote controller. During the transmit interrupt routine the microcomputer asserts its /ICB output, and will not accept any further interrupts until it has sent the status data to the remote controller. The TBRE output from the UART is routed through connector P1 pin 36 to the microcomputer I/O terminal 10 to identify the interrupt as a transmit routine. The serial output from the UART is output TR0 (pin 25) and is routed through line driver U3 to the remote controller through external connector A6A1W1J1.

Connections between the serial asynchronous interface module and the remote controller may be selected to accommodate signals compatible with MIL-188C/RS-232C, RS-423 and RS-422. The selection is made by connecting the remote controller to the interface external connector A6A1W1J1 in accordance with Table II (shown on the schematic) and using the links (on the Serial Asynchronous Interface module) in accordance with Table IV (shown on the schematic).

The interrupt circuitry on the A6A1 module not only generates the interrupt request, but it also provides the microcomputer with the interrupt vector. This is the program memory address at which the interrupt routine starts. A specific sequence of ROMC signals (put out when the CPU expects the interrupt vector address) is detected by gates U15D, U15A and flip-flops U16C, U16D and U16A. When these signals are received, gate U15A enables switches U13A and U14A to output the interrupt vector on the data bus to be read by the microprocessor.

4.3.9 Power Supply, A10

The receiver contains a power supply module that provides the power required for operation of the receiver. Refer to schematic diagram, Figure 7-12. The module operates from an ac line input, steps down the voltage, rectifies the ac, filters and regulates the various divided voltages. The unit contains a circuit card switch which provides for switching the transformer input for 100, 120, 220 or 240 volts ±10% operation from the input power line. This line frequency can be between 43 and 420 Hz and is controlled through the POWER-ON toggle switch located on the front panel. The input power is also fused through F1, located on the rear panel for easy access. The 100 or 120 volt input must be fused differently than the 220 or 240 volt input. The alternate fuse is contained in a fuse holder located inside the power supply.

4.3.9.1 DC Power Output

The secondary of transformer T1 contains three separate windings that provide the six different dc outputs for receiver operation. These six dc outputs, along with their tolerances are listed below:

+20 ±1 volt
+15 ±0.5 volt
+15 volts unregulated (nominally +22 volts)
−15 ±0.5 volt
+5 +0.5 −0.2 volts
+5 volts unregulated (nominally +10 volts)

Conventional bridge rectifiers CR1, CR2 and CR3 provide ac to dc rectification while capacitors C1, C4, C7 and C10 provide filtering and to smooth the pulsating dc. Capacitors C1 through C9 are connected adjacent to the three voltage regulators to suppress possible oscillations. The rectified and filtered dc from one winding 12 to 13 of the transformer is coupled to dc regulator A10A2, which provides the regulated +20 volts to pins 1 and 14 of A10J3. Winding 6 to 8 provides the +15 volts unregulated to pins 3 and 16, the +15 volts regulated through regulator U2 to pins 7, 8, 10, 11 and 24 and the −15 volts regulated through regulator U3 to pins 22 and 23. Winding 9 to 11 provides the +5 volts unregulated to pins 5 and 18 and the +5 volts regulated through regulator U1 to pins 2, 4, 15 and 17 of A10J3. The six dc outputs from A10J3 are routed to various applications throughout the receiver circuitry.

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SECTION V
MAINTENANCE

5.1 GENERAL

This section provides detailed procedures for conducting preventive maintenance, performance testing, fault isolation, and corrective maintenance on the RA6790/GM HF Receiver. The maintenance areas covered by these procedures include: inspection for damage and wear, cleaning and lubrication, performance tests, operational checkout and fault isolation, board level fault isolation, and receiver assembly and disassembly. Performance tests and Built-In Test Equipment (BITE) checkout procedures are presented in sufficient detail to allow fault isolation to the individual module/printed circuit board level. Routine application of preventive maintenance and performance test procedures will provide extended Receiver life, early indications of potential operating problems, and optimum Receiver performance. A recommended Preventive Maintenance Schedule is shown in Table 5-1.

TABLE 5-1. PREVENTIVE MAINTENANCE SCHEDULE

Procedure	Interval	Comments
Inspection for Damage or Wear	60 days	Interval variable depending on operating environment.
Cleaning	30 days	Interval variable depending on equipment use.
Lubrication	None	
Performance Tests	180 days	Interval variable depending on location/application requirements.

5.2 PREVENTIVE MAINTENANCE

The following paragraphs detail the preventive maintenance procedures to be used when servicing the RA6790/GM HF Receiver.

5.2.1 Inspection for Damage or Wear

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the Receiver is inoperative. At a minimum, the following items should be visually inspected.

1. Inspect the equipment covers and front panel for condition of finish and panel marking.
2. Inspect for dents, punctures, or warped areas.
3. Inspect quarter-turn fasteners and receptacles.
4. Inspect the external surfaces for loose or missing screws or washers.
5. Inspect the receptacles for condition of pins, contacts, and mounting.

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6. Inspect the internal components for signs of deterioration, discoloration, or charring. Check for melted insulation and damaged, cracked, or broken components.

7. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.

8. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

5.2.2 Cleaning and Lubrication

Cleaning

Cleaning should be performed to remove accumulated dust, grease, and other contamination, and to ensure trouble-free operation.

CAUTION

Avoid the use of chemical cleaning agents containing benzene, toluene, zylene, acetone, or similar solvents. These chemicals may damage the plastics used in this Receiver.

1. **Exterior** – Dust the cabinet off with a soft cloth. Dust the front panel controls with a small-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean, lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the front panel.

2. **Interior** – Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. Dust is best removed by dry, low-pressure air. Dirt clinging to surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton-tipped applicator for cleaning in narrow spaces and on the circuit boards.

3. **Switch Contacts** – When maintenance is necessary due to accumulated dirt and dust on the contacts, observe the following precautions: Clean the switch contacts with isopropyl alcohol or a mild detergent solution. Avoid cleaning solutions containing benzene, acetone, or similar solvents.

Lubrication

Lubrication is unnecessary in the Receiver. If the main tuning shaft appears to be binding during rotation in either direction, perform the following:

1. Disconnect receiver power source.

2. Loosen and remove the tuning knob.

3. Loosen the six (6) quarter-turn fasteners and remove the receiver top and bottom covers.

4. Remove the receiver front panel as directed in Paragraph 5.7, Assembly and Disassembly.

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5. Loosen both tuning-shaft retainer nuts (one located behind tuning knob, the other located behind tuning-shaft encoding wheel).

6. Retighten tuning-shaft retainer nuts finger tight only.

CAUTION

Overtightening tuning-shaft retainer nuts may cause damage to tuning assembly and the A9 module.

7. Reinstall tuning knob and flywheel and retighten screws.

8. Check for smooth, free operation of tuning knob.

9. Reinstall the receiver front panel as directed in Paragraph 5.7, Receiver Assembly and Disassembly.

10. Reinstall receiver top and bottom covers and retighten six (6) quarter-turn fasteners.

11. Reconnect power source.

5.3 MAINTENANCE SUPPORT EQUIPMENT

Certain procedures involved with both performance testing and board-level fault isolation may require the use of external test equipment to supplement BITE. Table 5-2 lists suggested test equipment by type and required operational characteristics. Not all test equipment listed is required for any one procedure. Equipment required for a particular test is specified in the procedure for that test.

TABLE 5-2. MAINTENANCE SUPPORT EQUIPMENT

Instrument	Specifications	Recommended Instrument or Equivalent
Digital Multimeter	Range: 0 to 150 Vac and dc 0 to 1A ac and dc Display: 3½ digits Accuracy: ±L.S. digit	Fluke 8000A-01
Oscilloscope, Dual Trace	Sensitivity: 5 mV/div. Frequency: dc to 2 MHz	Tektronix 465B
Oscilloscope, Probe	–	Tektronix P6105X10
RF Voltmeter	Range: 300 mV to 3 Vrms Frequency: 100 kHz to 70 MHz Input Impedance: > 1 M ohm with 50 ohm adapter	Boonton 92-B
Distortion Analyzer	Distortion Levels: 0.1 to 100% Frequency: 5 Hz to 600 kHz Voltage Range: 300 uV to 300 Vrms Voltage Accuracy: ±2% up to 300 kHz	Hewlett-Packard 331A

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TABLE 5-2. MAINTENANCE SUPPORT EQUIPMENT (Cont.)

Instrument	Specifications	Recommended Instrument or Equivalent
Digital Frequency Counter	Frequency Range: 0 to 50 MHz Sensitivity: 0.1 Vrms, 0.3 V pulse @ 8 ns min. p.w. Impedance: 1 M ohm Accuracy: 1 part in 10^6 ±1 count	Hewlett-Packard 5340A
Signal Generator	Frequency Range: 500 kHz to 100 MHz Accuracy: ±0.5% of dial setting Stability: < 10 parts in 10^6 Output Level Range: −140 dBm to ±10 dBm Modulation: AM −0 to 100% FM ±150 kHz @ 30 MHz Output Impedance: 50 ohms	Hewlett-Packard 8640B
RF Probe	–	Boonton 91-12F
50 ohm Adapter	–	Boonton 91-8B
Step Attenuator	–	Kay Electric 432-D
Headphone Set	600 ohm	Racal/Amplivox V31B
Audio Junction Box	–	Racal A08047
W-12 Cable Assembly	–	Racal C08556-2
Adapter	BNC Female to SMB Male	–
RF Test Cables, Standard	BNC Male, both ends, 5' length, quantity 4	–

5.4 RA6790/GM OPERATIONAL CHECKOUT AND FAULT ISOLATION PROCEDURE

Operational checkout of the RA6790/GM HF Receiver must be approached using a symptom/diagnostic analysis to augment the results of BITE test procedures. Since BITE is not a panacea for all electromechanical problems, a degree of interpretation is necessary by maintenance personnel. The scope of the analysis must include the conditions that preceeded the use of BITE in addition to those during and following its use. Interpretation of the results will, with a probability of greater than 90%, verify the operational readiness status of the Receiver or isolate a receiver fault to a specific board. Both verification and fault isolation depend upon careful observation of all symptoms starting with the initial step of energizing the Receiver. Further, for fault isolation, certain assumptions must be made in order to facilitate an intelligent assessment. These assumptions are: (1) the previous configuration of the Receiver is correct, i.e., filter complement installed correctly, system interfaces properly connected; (2) the Receiver was properly installed in an operational position (station); (3) the Receiver was functioning correctly prior to the occurance of the fault; and (4) all connections, connectors, cables and components had been checked for correct placement, continuity and tightness.

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The following procedures detail verification and fault isolation.

5.4.1 Initial Check

1. Verify that the PC wafer in A10 J1 on receiver rear panel matches available line voltage.

2. Energize Receiver by turning POWER ON switch to "ON" position.

3. Observe edge lighting and Liquid Crystal Displays (LCDs). If edge lighting is present and LCD displays contain data, there is a reasonable confidence factor (80%) that the Power Supply (A10) is working properly. Proceed to step 4.

   IF: a. Edge lighting is not present, the +15 volts from the A10 is malfunctioning. Check this voltage through to A10 and correct the malfunction.

   b. Edge lighting is present, frequency display contains mostly zeroes, and no mode indication is present, either the wafer does not match available line voltage, or the A6A2 Microcomputer Assembly is faulty and should be replaced.

4. Depress the LOCAL/REMOTE pushbutton switch on the front panel. The LCD display should indicate a change in receiver control from no display to REMOTE or vice versa. Repeated pressing of the LOCAL/REMOTE pushbutton switch should alternate the display between no display and REMOTE indications.

   IF: a. The Receiver indicates that it is in the REMOTE mode, and depressing the LOCAL/REMOTE pushbutton does not change the display, either the A6A2 Microcomputer Assembly or the A9 Front Panel Assembly is faulty and must be replaced.

   b. The receiver display does not indicate that it is in REMOTE, further isolation is possible. Depress the METER RF/AF pushbutton switch. The meter display should change correspondingly. If it does change, the REMOTE/LOCAL pushbutton switch is probably bad and the A9 Front Panel Assembly should be replaced. If the meter display does not change, initialize the Receiver by depressing the LOCK and AM pushbuttons simultaneously and allow the Receiver to initialize (approximately one minute). Once again attempt to change from LOCAL to REMOTE and back; and from RF to AF meter indications. If the display still will not change, the fault is probably on the A6A2 Microcomputer Assembly which should be replaced.

NOTE

Once steps 1 through 4 have been successfully accomplished, it can be assumed with 60% confidence that both the A6A2 Microcomputer and the A9 Front Panel Assemblies are functional. To increase the confidence factor, perform step 5.

5. Ensure that the Receiver is under LOCAL control (indicated by absence of REMOTE in LCD display). Depress the ENTER pushbutton switch momentarily, followed by

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numerals 12345678. These numerals should appear as 12.345678 on the frequency LCD. If this display is correct, then a confidence factor of 99% can be assumed regarding the total reliability of the A6A2 Assembly and a confidence factor of 60% for the A9 Assembly.

6. Ensure that the Receiver is under LOCAL control. If MAN is not displayed in LCD, momentarily depress the MAN pushbutton on the front panel to achieve Manual IF gain control. Once MAN is visible on the LCD, ensure that SHORT, MED, or LONG are not present in the display. If any of these three indications are present, momentarily depress the corresponding SHORT, MED, or LONG pushbutton on the front panel to remove the indication from the display.

When set up correctly, only the MAN display should be present in the LCD. Also, ensure that the meter indication is set for RF level. Once this condition has been attained, slowly rotate the IF GAIN potentiometer on the front panel from the full clockwise to full counter-clockwise positions and back again while observing the RF level meter display in the LCD. The RF level display should range from zero (no indication) to full scale and back again to zero. If this range is not attainable, then either the A4 Main IF Assembly (60% probability) or the A9 Front Panel Assembly (40% probability) is at fault and should be replaced.

NOTE

Failure to attain the desired range definitely indicates that proceeding with the BITE checks is useless until the problem is corrected. On the other hand, full range indication demonstrates that the A4 Main IF measurement system used by BITE is functional and BITE checks will yield useful results.

Since steps 1 through 6 are prerequisite to successful BITE testing, BITE may now be effectively applied.

5.4.2 BITE Check

1. Ensure that the initial Check Procedures (Paragraph 5.4.1) have been successfully accomplished.

2. Momentarily depress the LOCK and AM pushbuttons on the front panel. The Receiver will enter its BITE check mode as indicated by (1) the appearance of REMOTE in the LCD display; (2) the rapidly changing frequencies, modes, and LCD displays on the front panel, and (3) the presence of rapidly changing AF tones and sounds (if AF is being monitored). BITE performs checkout procedures on the following assemblies:
   A2 – First Mixer
   A3 – Second Mixer
   A4 – Main IF/AF
   A5 (if installed) – ISB
   A6A2 (memory portion) – Microcomputer
   A7 – First and Third LO Synthesizers
   A8 – Second LO Synthesizer
   IF Bandwidth Filters

NOTE

By observing the frequency display LCD, it is possible to isolate a fault to the board level by noting BITE error code(s) which appear in that display.

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3. If an error code does appear in the frequency LCD (this will consist of a two-digit number) refer to Table 5-3, BITE Error Code Identification. If more than one board is identified as a suspected fault, depress and release the LOCK and CW pushbuttons simultaneously and observe the display. A subsequent number will appear which, when considered along with the number which first appeared should identify the faulty board.

4. Replace the faulty board and repeat steps 1 through 3 until no further faults are indicated by BITE. (This will be indicated by the exit from REMOTE and the return of the Receiver to its pre-BITE status.)

Successful completion of Paragraphs 5.4.1 and 5.4.2 verify the operational readiness status of all boards except:
A1 Low Pass Filter
A6A1 Remote Interface
Audio portions of A4 Main IF/AF and A5 ISB (if installed)

TABLE 5-3. BITE ERROR CODE IDENTIFICATION

Displayed Error	Description	Probable Fault
01	First Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A7
02	Second Local Oscillator (reference) synthesizer not locked.	A8
03	First Local Oscillator synthesizer does not break lock to enter fast sampling mode on 500 kHz step change.	A7
04	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A8
05	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz and 500 Hz step change, respectively. 03 and 05 indicates A7 fault; 04 & 05 by itself indicates A8 fault.	A8, A7
06	Filter slot one contains a symmetrical filter, but there is/are SSB filter(s) also in the system.	Wrong or bad filter.
07	Filter slot one contains an upper sideband filter. ISB operation, if installed, will be impaired.	Wrong or bad filter.
08	No USB filter has been found in the system, and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
09	Too many symmetrical filters installed in the system.	Check filters installed.
10	Not used.	

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TABLE 5-3. BITE ERROR CODE IDENTIFICATION (Cont.)

Displayed Error	Description	Probable Fault
11	No LSB filter has been found in the system and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
12	No symmetrical filters have been found in the system.	Wrong or bad filter.
13	Filter slot one does not contain a lower sideband filter, but ISB is installed. If ISB is installed and no 13 error, A5 is functional.	Wrong or bad
14	Ramdom access memory test failure: Data written to memory different from data read back.	A6A2
15	Either no filters are installed in the system, or the synthesizer signal strength is out of range prescribed for BITE. NOTE If no 15 error, A2, A3, and A4 are fully functional.	A2
16	Filter slot one contains no filter.	Wrong or bad filter.
17	Two or more LSB filters have been found in the system.	Wrong or bad filters.
18	Two or more USB filters have been found in the system.	Wrong or bad filters.
19	Although a lower sideband filter has been found in this system, it is not installed in filter slot one. ISB operation, if installed, will be impaired.	Wrong or bad
20	Not used.	
21	Filter in filter slot one is skewed from the IF center frequency.	*Wrong or bad filter.
22	Filter in filter slot two is skewed from the IF center frequency.	*Wrong or bad filter.
23	Filter in filter slot three is skewed from the IF center frequency	*Wrong or bad filter.
24	Filter in filter slot four is skewed from the IF center frequency.	*Wrong or bad filter.
25	Filter in filter slot five is skewed from the IF center frequency.	*Wrong or bad filter.

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TABLE 5-3. BITE ERROR CODE IDENTIFICATION (Cont.)

Displayed Error	Description	Probable Fault
26	Filter in filter slot six is skewed from the IF center frequency.	*Wrong or bad filter.
27	Filter in filter slot seven is skewed from the IF center frequency.	*Wrong or bad filter.
28	Not used.	
29	Not used.	
30	Not used.	
	NOTE 31 through 37; 80% probability of bad filter. 30% probability A4 board.	
31	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot one.	Bad filter, A4
32	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot two.	Bad filter, A4
33	BITE frequency sweep underflowed while attempting to measure bandwidth of filter in filter slot three.	Bad filter, A4
34	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot four.	Bad filter, A4
35	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot five.	Bad filter, A4
36	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot six.	Bad filter, A4
37	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot seven.	Bad filter, A4

*Synthesizers off frequency or wrong or bad filters.

5.4.3 A1 Low Pass Filter Check

1. Connect a suitable antenna to the RF IN jack, J1 on the receiver rear panel.
2. Tune the Receiver to a known local AM broadcast station.

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3. Verify reception of the signal by connecting a suitable speaker or headphones. If the station is not heard (confirm that the station is on the air), observe the RF level meter on the Mode LCD. If the signal strength meter (RF level) has no level indication, the A1 Low Pass Filter Module is defective and should be replaced.

5.4.4 A4 Main IF/AF (AF Section) Check

If the RF level meter indicates a signal is present as specified in Paragraph 5.4.3, adjust the front panel MAIN LINE LEVEL potentiometer (screwdriver - set) to determine if the signal can be observed at Line 1 out (J3). If the signal cannot be found the A4 Main IF/AF board (AF portion) is faulty and the A4 must be replaced.

5.4.5 A5 ISB (AF Section) Check (if installed)

Tune to a known local AM station. Depress the ISB pushbutton and listen for the presence of the signal. If the signal cannot be heard, adjust the ISB LINE LEVEL potentiometer (screwdriver adjust) on the front panel to determine if the signal can be heard or observed at Line 1 or Line 2 out (J3). If not found, the A5 ISB (AF portion) is faulty and A5 must be replaced.

5.4.6 A6A1 Remote Serial Asynchronous Interface Check(if installed)

1. Ensure that all previous paragraphs have been successfully accomplished.

2. Connect a suitably wired remote terminal to the Receiver via connector A6A1W1J1 on the rear panel.

3. Enter S99GCR on the terminal keyboard and observe the results on the remote display. If data is displayed, A6A1 is functional. If data is not displayed, A6A1 is faulty and must be replaced.

NOTE

99 represents the receiver number. If the receiver number is different, enter the desired number instead of 99.

This completes the Operational Checkout and Fault Isolation Procedures for the RA6790/GM Receiver.

5.5 RA6790/GM PERFORMANCE TESTS

RA6790/GM performance tests can be most effectively carried out if the technician gains some degree of familiarization with the operating instructions and circuit descriptions provided in Sections III and IV, respectively. Parts lists and component location diagrams are located in Section VI.

These performance test procedures may be used for initial inspection, periodic checks and to confirm performance specifications after repairs have been made. These tests determine Synthesizer performance, Audio Power and Distortion, Gain Modes, and Final IF Frequency. The tests should be conducted only by skilled technicians using the equipment listed in Table 5-2.

All tests should be conducted using Figure 5-1 as a standard test set-up. Equipment should be allowed a warm-up period of at least 30 minutes prior to conducting the test. If the Receiver does not satisfactorily pass a test, refer to Paragraph 5.6, Board Level Fault Isolation.

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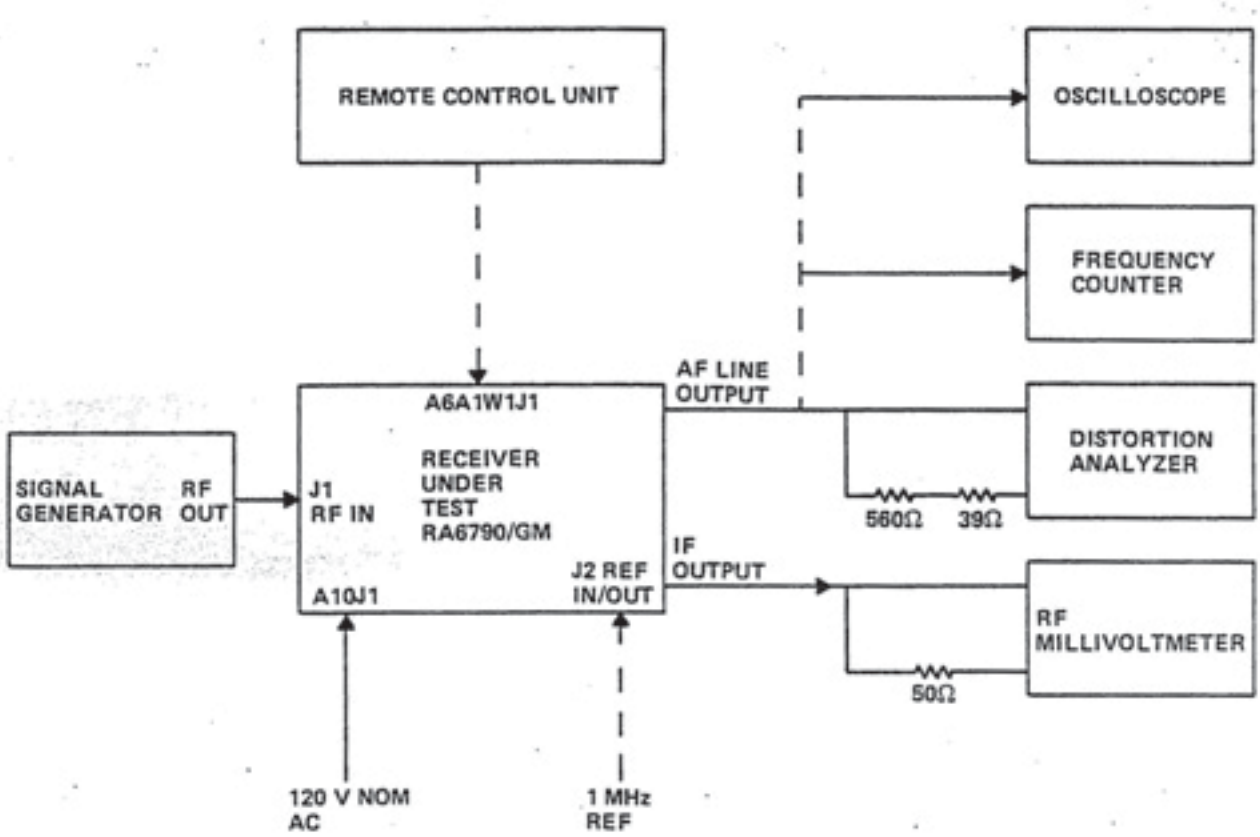

Figure 5-1. Standard Test Equipment Configuration

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5.5.1 Frequency Tuning

1. Connect the Receiver and test equipment as shown in Figure 5-1.

2. Set the Receiver as follows:
   a. Frequency — As required in Table 5-4
   b. Mode — CW
   c. BFO — 1000 Hz
   d. AGC — Short
   e. Bandwidth — 5 kHz (or closest bandwidth available)

3. Set the signal generator as follows:
   a. Frequency — As required in Table 5-4
   b. Level — −60 dBm, unmodulated

4. Set the Receiver and generator to the frequencies listed in Table 5-3. Ensure that the output frequency indicated by the counter remains within the limits 1 kHz ±10 Hz at each setting.

TABLE 5-4. TUNED FREQUENCIES

Receiver/Generator Tuned Frequency	AF Output
00.500000 MHz	1000 ±10 Hz
01.000000	1000 ±10 Hz
11.111111	1000 ±10 Hz
22.222222	1000 ±10 Hz
23.333333	1000 ±10 Hz
24.444444	1000 ±10 Hz
25.555555	1000 ±10 Hz
26.666666	1000 ±10 Hz
27.777777	1000 ±10 Hz
28.888888	1000 ±10 Hz
29.999999	1000 ±10 Hz

5.5.2 Frequency Display

1. Set up the equipment as in Figure 5-1.

2. Set the signal generator as follows:
   a. Frequency — 1.5 MHz
   b. Mode — CW
   c. Level — −100 dBm

3. Tune the Receiver to 1.5 MHz using manual gain mode, 3.24 kHz BW; CW; at −1.8 kHz BFO offset.

4. Ensure that frequency readout display is clearly visible from a distance of 3 feet.

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5. Ensure that is is possible to tune another frequency in the same frequency band.

6. Select tuning LOCK and ensure that frequency is not changed by further rotation of tuning knob.

5.5.3 Frequency Stability

1. Connect the frequency counter to the output of REF IN/OUT J2.

2. Ensure that the output frequency is 1 MHz ±1 Hz.

5.5.4 Frequency Calibration Resolution

Connect the frequency counter to internal standard (A8TP10).

Ensure that the internal standard is 5 MHz ±1 Hz.

5.5.5 RF Gain Control

1. Set up the equipment as in Figure 5-1.

2. Set the Receiver controls as follows:
   a. Power — ON
   b. Gain Mode — Manual
   c. Detection Mode — CW
   d. BW — 3.24 kHz

3. Set the signal generator for an output of 1.5 MHz at −100 dBm, CW. Connect the signal generator to RF IN connector J1 on rear panel.

4. Using the remote controller, adjust the manual gain control on the Receiver fully clockwise and adjust the line level control for 1 mW output on distortion analyzer.

5. Adjust the manual gain control on the remote control device one step down and check whether or not the AF output falls by 3 ±1.5 dB.

6. Increase signal generator level to 1 mW and repeat step 5 until manual gain is at minimum.

7. Restore the 1 mW reference at the minimum manual gain and note the signal generator level. This should be greater than −10 dBm.

5.5.6 Final IF Frequency

1. Set up the equipment as shown in Figure 5-1.

2. Set the Receiver controls as follows:
   a. Power — ON
   b. Gain Mode — AGC-SHORT
   c. BW — 3.2 kHz
   d. Receiver Tuned Frequency — 1.5 MHz
   e. Detection Mode — CW

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3. Set the signal generator for an output of 1.5 MHz, CW at a level of −100 dBm.

4. Note the IF output level indicated on the RF voltmeter.

5. Remove the 50 ohm load from the IF output and observe that the indicated output voltage increases by 6 dB ±1 dB.

6. Connect the frequency counter to IF output jack J2 and measure the IF frequency. This should be 455.000 kHz.

5.5.7 Fixed and Variable BFO Operation

1. Set the receiver controls as follows:
   a. Power — ON
   b. Gain Mode — N/A
   c. Detection Mode — CW
   d. BW — N/A
   e. BFO — ON (word BFO displayed in Mode LCD)

2. Disconnect the A4 module by removing W10P1.

3. Connect the frequency counter to A4J6 to monitor the BFO frequency.

4. Using the receiver front panel controls, select each BFO indication listed in BFO Indicator column of Table 5-5 and verify the frequencies listed in BFO Frequency Column are obtained.

5. Select USB and LSB modes and observe the BFO frequency is 455.000 kHz. (SSB/ISB receivers fitted with 08409 and 08410 option filters only.)

6. Disconnect frequency counter and reconnect W10P1 to A4 module.

TABLE 5-5. BFO Test Values

BFO Indicator	BFO Frequency
0.00 kHz	455.000 kHz
+1.11	453.890
2.22	452.780
3.33	451.670
4.44	450.560
5.55	449.450
6.66	448.340
7.88	447.120
7.99	447.010
−1.11	456.110
−2.22	457.220
−3.33	458.330
−4.44	459.440
−5.55	460.550
−6.66	461.660
−7.77	462.770
−7.88	462.880
−7.99	462.990

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5.5.8 Audio Output Power

1. Set up test equipment as shown in Figure 5-1.

2. Set receiver controls as follows:

a.	Power	ON
b.	Gain Mode	AGC-SHORT
c.	BW	3.24 kHz
d.	Detection Mode	CW
e.	Receiver Tuned Frequency	1.5 MHz

3. Set the signal generator for an output of 1.5 MHz at –97 dBm, CW.

4. Tune the signal generator (or receiver) to produce an AF output of 1.8 kHz ±50 Hz as indicated on the Frequency Counter.

5. Set the AF output level to 1 milliwatt using the LINE LEVEL control on the receiver front panel and phone output.

6. Select receiver bandwidth of 6.8 kHz and AM detector mode. Amplitude modulate the input signal 30% at 1 kHz.

7. Observe that the AF output level is within 5 dB of the reference set in step 5 for both line output and phone output.

8. Slowly rotate the AF gain control through the control range. Observe that the phone output level varies smoothly over the full control range.

5.5.9 Audio Distortion

1. Set up the equipment as shown in Figure 5-1.

2. Set receiver controls as follows:

a.	Power	ON
b.	Gain Mode	Manual Gain
c.	Detection Mode	CW
d.	BW	3.24 kHz
e.	BFO	–1.00 kHz
f.	Receiver Tuned Frequency	1.5 MHz

3. Set the signal generator for an output of 1.5 MHz at –47 dBm, CW.

4. Adjust manual gain control for 1 mW output. Measure distortion. Distortion should be less than 2%.

5. Connect phone output from receiver front panel to distortion analyzer and adjust phone output for 10 mW. Measure distortion. Distortion should be less than 3%.

5.5.10 Operation After Restoration of Power

1. Carefully note the receiver tuned frequency, BW and other displayed functions on receiver front panel and de-energize the Receiver.

2. After ½ hour energize the Receiver and ensure that the Receiver returns to the display noted in step 1.

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5.6 BOARD LEVEL FAULT ISOLATION

Figure 5-2 shows signal flow between individual circuit cards, and the jacks and/or test points for measuring signal values. This information, along with the BITE check detailed in Paragraph 5.4.2 and the Performance Tests detailed in Paragraph 5.5 should be used in isolating malfunctions to the board level. Receiver settings, signal generator settings, and connector pin location diagrams are shown as part of Figure 5-2. The following procedures should be used to perform signal level tests:

1. Set signal generator outputs as specified in Figure 5-2.
2. Set receiver front panel controls as specified in Figure 5-2.
3. Measure values indicated at each jack or test point using appropriate test equipment.
4. Tolerances are: ±3 dBm; ±0.5 volts.

Once a fault has been isolated, the faulty circuit card should be replaced in accordance with the Receiver Assembly and Disassembly procedures detailed in Paragraph 5.7; and receiver proper operation verified. Verification is accomplished by performing BITE check (Paragraph 5.4.2) and Performance Tests (Paragraph 5.5).

5.7 RECEIVER ASSEMBLY AND DISASSEMBLY PROCEDURES

The following paragraphs outline the procedures for removal and installation of the individual circuit card assemblies used in the RA6790/GM HF Receiver. A complete list of these assemblies is contained in SECTION VI, Replacement Parts List, of this instruction manual.

5.7.1 Preliminary Procedure

Prior to removing or installing any assembly it is necessary to disconnect the Receiver from its power source. It is also necessary to remove the Receiver from the system (except to replace the fuse).

NOTE

Ensure that all system cables are disconnected from the Receiver prior to removing the Receiver from its mounts. Place the Receiver on a suitable work space large enough to allow for positioning the Receiver either horizontally or vertically as required for removal of the desired board. The only tools required for LRU removal or installation are a flat-blade screwdriver and a screw starter. Adequate light should be available for ease in reading internal cable, jack, and connector numbers, and for aligning LRU mounting holes with corresponding mounting fixtures on the receiver chassis.

CAUTION

Do not expose the Receiver to direct ultraviolet light while performing the following steps. Such exposure may cause erasure of data stored in the EPROMS.

5.7.2 Top and Bottom Covers

If boards A2, A3, A7, or A8 are to be removed or installed, only the receiver's bottom cover must be removed for access. If boards A4, A5, A6A1, A6A2 or A10 are to be removed or installed,

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only the receivers top cover must be removed for access. If boards A1 or A9 are to be removed or installed, both the receiver's bottom and top covers must be removed for access. The procedure for removing either cover is as follows:

1. Position the Receiver horizontally so that the cover to be removed is up.
2. Loosen (counterclockwise) the six (6) ¼ turn fasteners located on the cover.
3. Carefully lift the cover by its edges and remove it from the Receiver.

Installation of either cover is as follows:

1. Position the cover on the Receiver so that the six (6) ¼ turn fasteners on the cover align with their mounting holes on the Receiver, and so that the front edge of the cover is inserted into the slot on the rear of the front panel.
2. Apply a small amount of hand pressure to the cover to engage the fastener with its mount.
3. Tighten (clockwise) the six (6) fasteners ¼ turn.

5.7.3 A1 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove both the receiver top and bottom covers as directed in Paragraph 5.7.2.
3. Disconnect SMB connector A1W2P1 from J5 on the receiver frame.
4. Disconnect BNC connector A1W1J1 from J1 (the RF IN jack) on the rear panel.
5. Stand the Receiver on its side.
6. Working from the bottom of the Receiver, loosen and remove the two screws and hardware from the ends of the A1 module.

CAUTION

Do not allow the A1 module to drop when the screws are removed. Failure to do so may cause damage to the A1 module or to the Receiver.

7. Carefully lift out the A1 module from the top of the Receiver.

5.7.4 A1 Module Installation

Installation is the reverse of removal with the following notes:

1. The end of the A1 module marked "IN", when positioned correctly, is mounted on the mount nearest S2 (EXT-INT REF switch).
2. When installing the mounting screw at the "IN" end, ensure that the ground lug on the A1W1J1 cable is placed inside the A1 module between the A1 cover and the threaded mount, and that the mounting screw goes through the lug.

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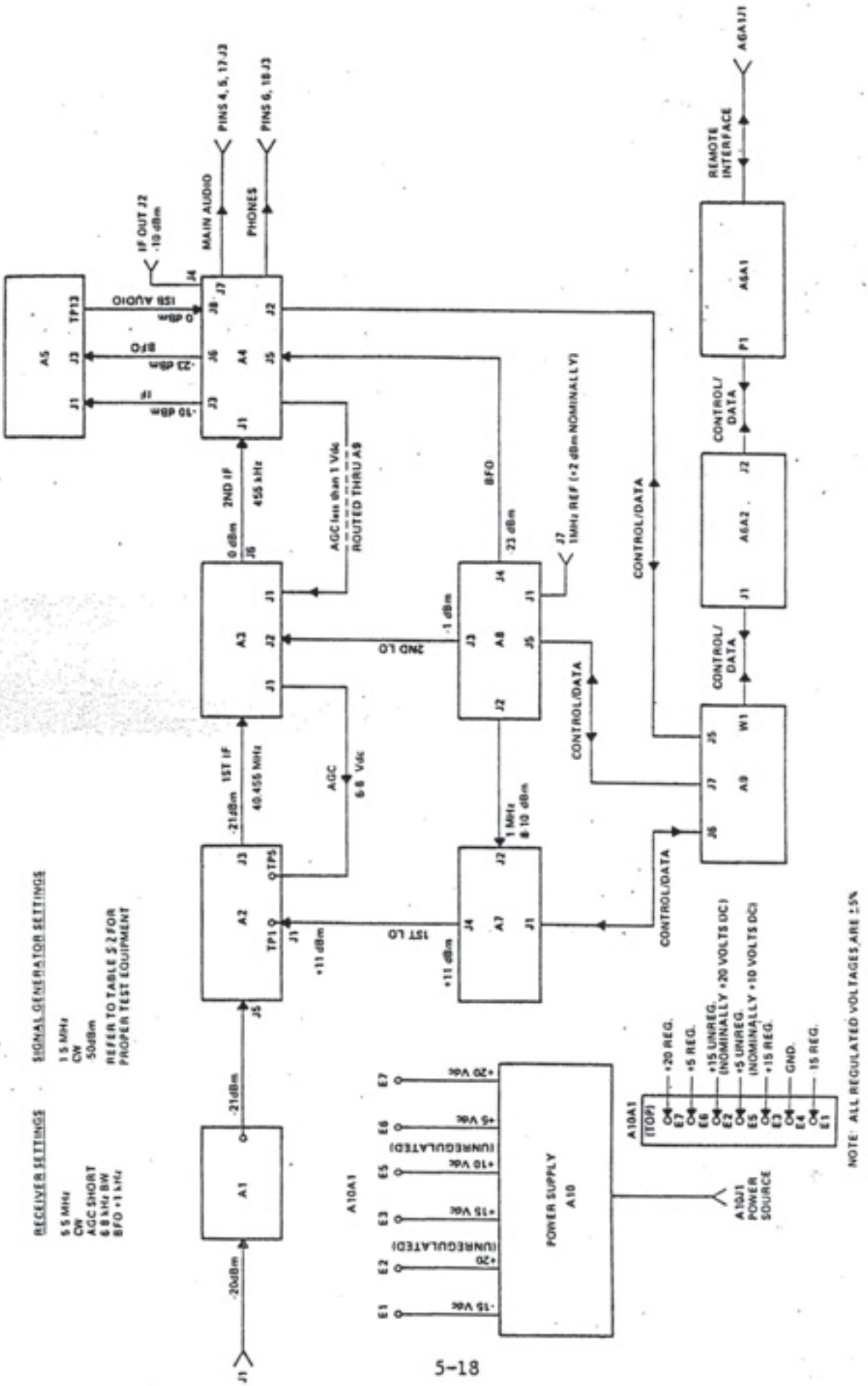

Figure 5-2. Typical Signal Levels, RA67U/GH HF Receiver

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5.7.5 A2 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver bottom cover as directed in Paragraph 5.7.2.
3. Remove the six (6) screws and hardware which holds down the A2 module cover.
4. Remove the A2 module cover.
5. Disconnect eight-pin connector W21P1 from A2J2.
6. Disconnect SMB connector W2P1 from A2J1.
7. Disconnect SMB connector W1P1 from J5 on the receiver frame.
8. Disconnect SMB connector A3W1P1 from A2J3.
9. Loosen and remove the six (6)screws and hardware which hold down the A2 module.
10. Lift out the A2 module tipping it slightly to avoid bumping the module against J5 and the four (4) feed-through capacitors located on the side of the receiver frame.

CAUTION

Bumping J5 or the capacitors may cause damage to the A2 module printed circuit track or components.

5.7.6 A2 Module Installation

Installation of the A2 module is the reverse of removal with the following notes:

1. Ensure cable W2P1 is located near the notch in the receiver frame when installing the module.
2. Ensure that the cable connected to W2P1 (coming from the A7 module area) is routed through the notch on the edge of the receiver frame. Failure to do so may result in damage to the cable.

5.7.7 A3 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver bottom cover as directed in Paragraph 5.7.2.
3. Using the pull-tab on the A3 module cover, carefully remove the A3 cover.
4. Disconnect eight-pin connector W22P1 from A3J1.
5. Disconnect SMB connector A3W2P1 from J6 on the receiver frame.
6. Disconnect SMB connector W4P1 from A3J2.
7. Loosen and remove the six (6) screws and hardware which hold down the A2 module cover.

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8. Remove the A2 module cover.

9. Disconnect SMB connector A3W1P1 from A2J3 on the A2 module.

10. Loosen and remove the six (6) screws and hardware which hold down the A3 module.

11. Lift out the A3 module tipping it slightly to avoid bumping the module against J2 and the five (5) feed-through capacitors located on the side of the receiver frame.

CAUTION

Bumping J6 or the capacitors may cause damage to the A3 module printed circuit track or components.

5.7.8 A3 Module Installation

Installation of the A3 module is the reverse of removal with the following note:

NOTE

Ensure cable A3W1P1 is located near the notch in the receiver frame when installing the module.

CAUTION

Ensure cable A3W1P1 is routed through the notch in the frame prior to installation of both the A2 and A3 module covers. Failure to do so may result in damage to the cable.

5.7.9 A4 Module Removal

1. Perform the Preliminary Procedures as directed in Paragraph 5.7.1.

2. Remove the receiver top cover as directed in Paragraph 5.7.2.

3. Remove the Bandwidth Filter cover and Bandwidth filters as directed in Paragraph 5.7.25.1.

4. Disconnect SMB connector W1P2 from A4J1.

5. Disconnect SMB connector W11P1 from A4J3.

6. Disconnect SMB connector W12P1 from A4J4.

7. Disconnect SMB connector W6P2 from A4J5.

8. Disconnect SMB connector W10P1 from A4J6.

9. Disconnect ribbon connector A5W1P1 from A4J8.

10. Disconnect ribbon connector W16P1 from A4J7.

11. Disconnect ribbon connector W15P1 from A4J2.

12. Loosen and remove the twelve (12) screws and hardware which hold down the A4 module.

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NOTE

The two (2) screws which hold down transformer T1 to the A4 module do not need to be removed to remove the module nor does the screw through U27. Eight (8) hold down screws are located around the A4 module edges, and the two (2) additional screws are located in the middle area of the module.

13. Lift out the A4 module.

5.7.10 A4 Module Installation

Installation of the A4 module is the reverse of removal with the following note:

NOTE

When positioning the A4 module for installation, the Bandwidth Filter slots (labelled FL1-FL7 on the A4 module) are located toward the side of the Receiver nearest the A10 (Power Supply) module.

CAUTION

Ensure that all cables and connectors are clear of the A4 module during installation. Failure to do so may result in having to remove the module again to properly position the cables.

5.7.11 A5 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver top cover as directed in Paragraph 5.7.2.
3. Disconnect ribbon connector A5W1P1 from A4J8.

NOTE

The connector disconnects from the A4 module, not the A5 module, and the ribbon cable is part of the A5 module.

4. Disconnect SMB connector W10P2 from A5J3.
5. Disconnect SMB connector W11P2 from A5J1.
6. Loosen and remove the four (4) mounting screws and hardware from the four corners of the A5 module.
7. Lift out the A5 module.

5.7.12 A5 Module Installation

Installation of the A5 module is the reverse of removal.

5.7.13 A6 Module Removal

1. Perform the Preliminary Procedures as directed in Paragraph 5.7.1.

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2. Remove the receiver top cover as directed in Paragraph 5.7.2.

3. Disconnect ribbon connector A9W1P2 from A6J1.

4. From outside the rear panel, loosen and remove the two (2) screws and hardware that hold A6A1WIJ1 to the rear panel.

5. Loosen and remove the six (6) screws and hardware that hold the upper edge of the A6 module to the side of the Receiver.

NOTE

On some Receivers, the second screw from the rear of the Receiver should be removed last. Behind this screw, between the A6A1 module and the receiver frame, is a nylon washer (insulator) that must not be lost. Inspect this screw prior to removal to determine if the Receiver has a washer at this location.

CAUTION

If the Receiver has a nylon washer, failure to reinstall it may cause damage to the A6A1 module.

6. Carefully lift out the A6 module.

NOTE

The A6 module is composed of two separate printed circuit boards, A6A1 and A6A2, joined in the middle by A6P1 which is a fifty (50) pin connector. If it is desired to separate the two boards, grasp one board in each hand and carefully pull them straight apart.

CAUTION

Failure to exercise care may result in damage to the connector.

CAUTION

After removing the A6A2 module, do not place it on a conductive surface as this may cause damage to the battery on the A6A2 module.

5.7.14 A6 Module Installation

Installation of the A6 module is the reverse of removal with the following notes:

CAUTION

When joining A6A1 and A6A2 together, ensure that the P1 connector holes and pins are correctly aligned with each other prior to applying pressure. Failure to do so may result in damage to the connector.

1. When installing the A6 module into the Receiver, ensure that A6A1W1J1 is located in the cutout on the rear panel, and the bottom edge of the module is in the nylon track on the receiver frame.

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2. For ease of installation, install the second screw from the rear panel with its nylon washer if installed (between the A6A1 module and the mounting post) first.

CAUTION

Failure to install the nylon washer (insulator) may cause electrical damage to the A6 module.

5.7.15 A7 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver bottom cover as directed in Paragraph 5.7.2.
3. Loosen and remove the single screw and hardware that holds down the A7 module cover.
4. Using the pull-tab on the A7 module cover, remove the A7 module cover.
5. Disconnect ribbon connector W13P1 from A7J1.
6. Disconnect SMB connector W3P1 from A7J2.
7. Disconnect SMB connector W2P2 from A7J4.
8. Loosen and remove the eleven (11) screws and hardware, and the nylon mounting post (from which the A7 module cover screw was removed in Step 3 above) which holds down the A7 module.

NOTE

The screw through A7U39 is not a module holddown screw. The screw through regulator A7Q4 is a module holddown screw. When removing the screw through A7Q4, take care not to lose the mica insulator which fits between A7Q4 and the A7 module.

CAUTION

Do not overtighten the screw through A7Q4 voltage regulator. Overtightening the screw may cause failure of the regulator.

9. Lift out the A7 module.

5.7.16 A7 Module Installation

Installation of the A7 module is the reverse of removal with the following notes:

1. When positioning the A7 module for installation, ensure that ribbon connector A751 is located next to the cutout in the receiver frame.
2. When installing the screw through A7Q4, ensure that the mica insulator is present between A7Q4 and the A7 module, and is centered on the mounting hole.

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CAUTION

Failure to insulate the screw through A7Q4 from A7Q4's metal pack with the mica insulator may cause electrical damage to the A7 module.

5.7.17 A8 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver bottom cover as directed in Paragraph 5.7.2.
3. Using the pull-tab on the A8 module cover, remove the A8 module cover.
4. Disconnect ribbon connector W14P1 from A8J5.
5. Disconnect SMB connector W7P1 from A8J1.
6. Disconnect SMB connector W6P1 from A8J4.
7. Disconnect SMB connector W3P2 from A8J2.
8. Disconnect SMB connector W4P2 from A8J3.
9. Remove the eight (8) screws and hardware which hold down the A8 module.
10. Lift out the A8 module.

5.7.18 A8 Module Installation

Installation of the A8 module is the reverse of removal with the following note:

NOTE

When positioning the A8 module for installation, ensure that ribbon connector jack J5 is located next to the cutout in the receiver frame.

CAUTION

Before installing the A8 module cover, ensure that all cables entering the A8 area are routed through their cutouts in the receiver frame. Failure to do so may result in damage to the cables.

5.7.19 A9 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove both the receiver top and bottom covers as directed in Paragraph 5.7.2.
3. Disconnect ribbon connector A9W1P2 from A6J1.

NOTE

The disconnection is made at the A6 module and the ribbon cable is part of the A9 module.

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4. Disconnect ribbon connector W13P2 from A9J6.

5. Disconnect ribbon connector W15P2 from A9J5.

6. Disconnect ribbon connector W19P1 from A9J4.

7. Disconnect ribbon connector W14P2 from A9J7.

8. Disengage the two friction locks on connector W20P1 and unplug the connector from A10J2 on the A10 module.

9. Stand the Receiver vertically on its rear panel. Loosen and remove the four (4) screws and hardware on the outside of the front panel which hold the front panel to the receiver frame.

10. Using the handles on the front panel, lift the front panel (A9 module) off the Receiver being careful not to snag connector W20P1 or its cable on the Bandwidth Filter cover. Snagging W20P1 may result in damage to the connector, the cable, or the POWER ON/OFF switch. If further disassembly is required, proceed to step 11.

11. Loosen and remove the single screw and hardware which holds down the tuning shaft encoding wheel.

12. Carefully remove the encoding wheel.

CAUTION

Do not pry on the encoding wheel, as the hidden side of the encoding wheel is part of the manual tuning encoder. Damage to the encoding wheel may impair manual tuning.

13. Rest the front panel on the front panel handles.

14. Remove first the lockwasher and then the flatwasher that fit between the encoding wheel and the tuning shaft.

15. Using fingers, loosen and remove the tuning shaft assembly retaining nut, lockwasher, flat washer, and nylon washer (insulator).

16. Loosen and remove the ten (10) screws and hardware which hold the A9 module to mounting posts on the front panel.

17. While gently lifting the A9 module, carefully work the keypad ribbon leads out of connectors A9J2 and A9J3.

NOTE

Connectors A9J2 and A9J3 are soldered to the A9 module. The keypad ribbon leads have no connectors fastened to them. To separate the ribbon leads from the connectors, use fingers to carefully pull the ribbon leads straight out.

18. Carefully fold the A9 module down away from the ribbon leads to expose the wires leading to the front panel controls.

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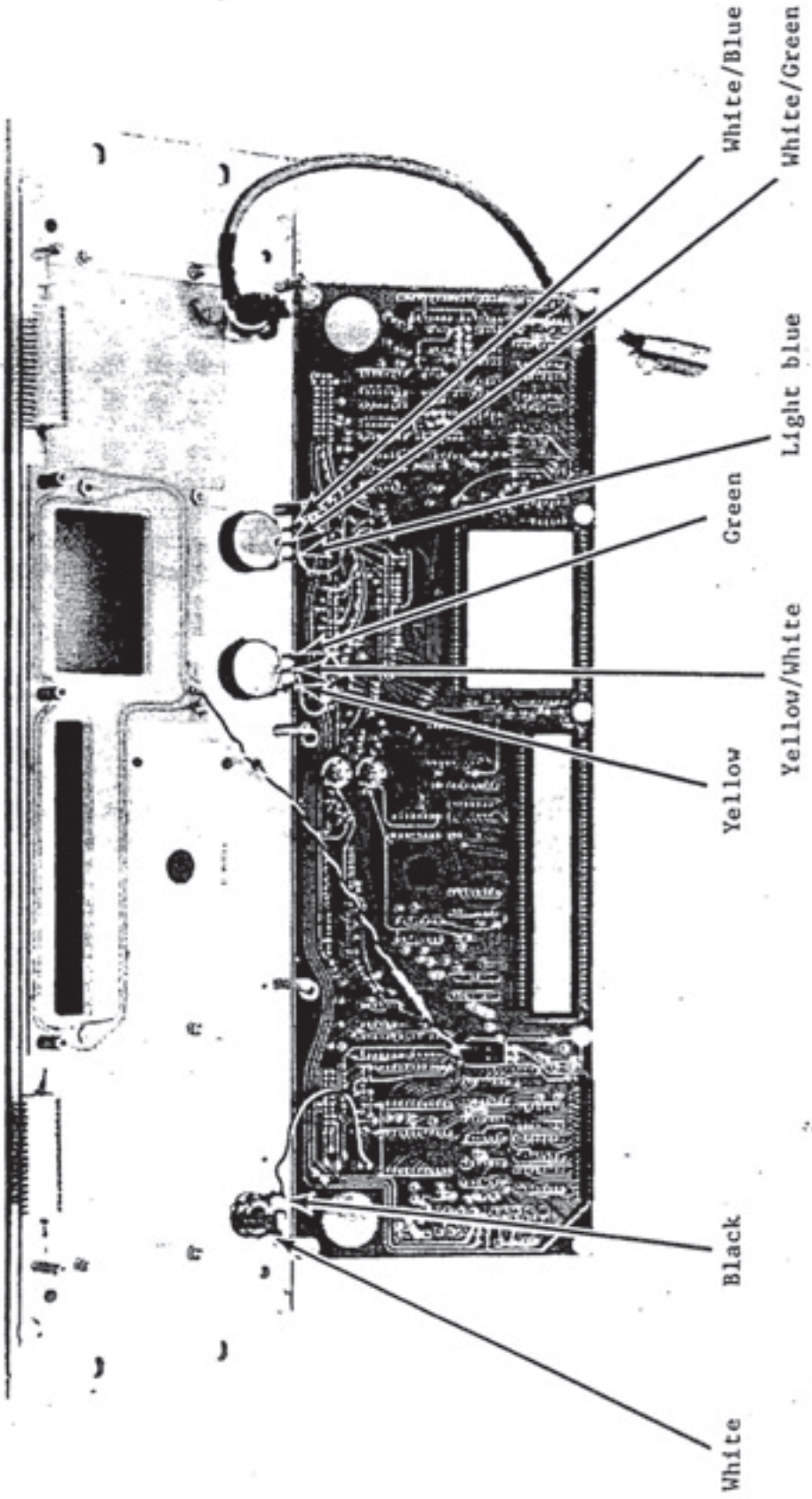

Figure 5-3. Wiring Detail, A9 Circuit Card Assembly

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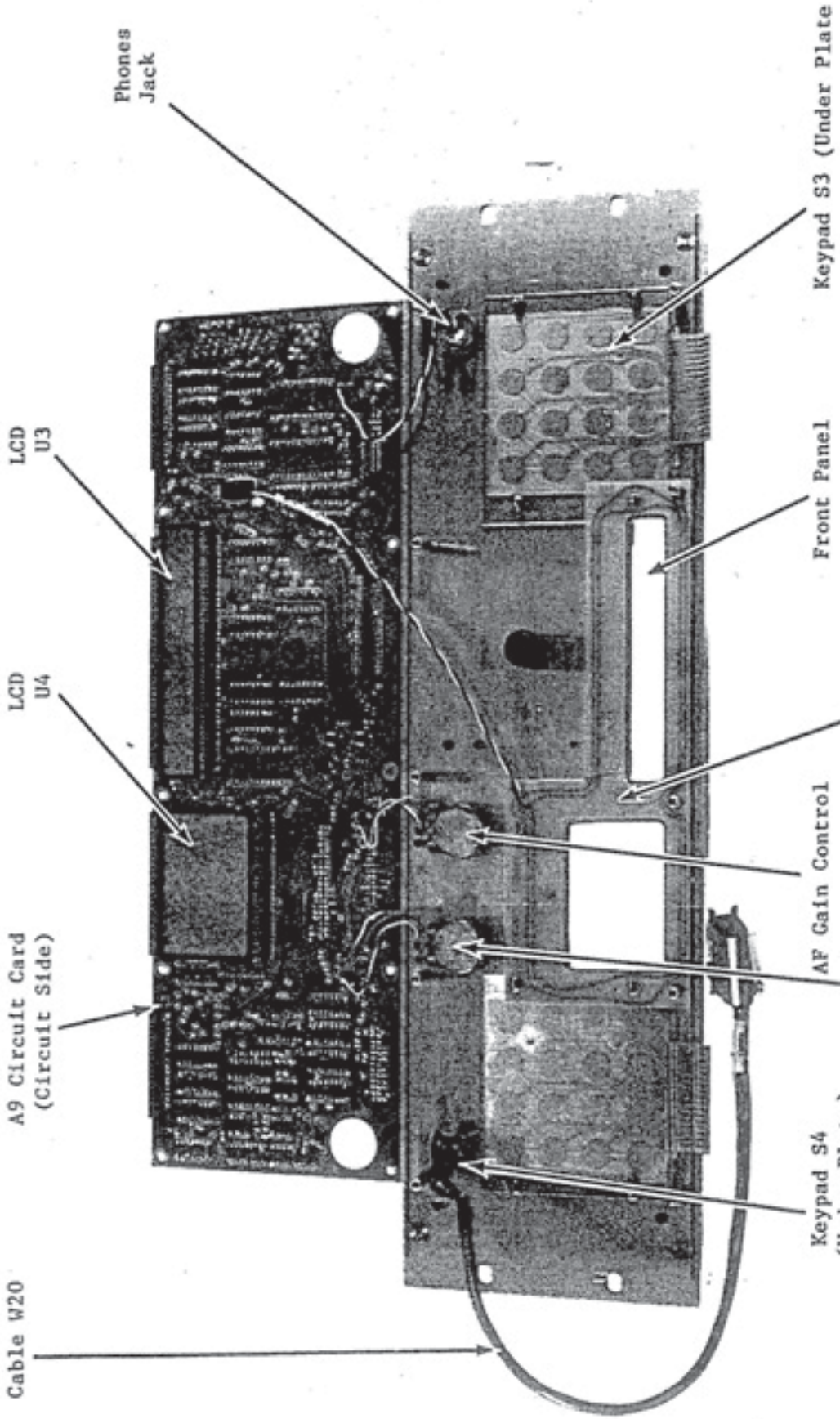

Figure 5-4. Front Panel Assembly, Partially Disassembled

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CAUTION

Be careful when folding back the A9 module not to pull out any wires which lead to the controls. Also be careful not to damage the Liquid Crystal Display (LCD) units, or the Fault Indicator Light Emitting Diode (LED).

19. Disconnect three pin connector W1P1 from A9J8 on the A9 module. Refer to Figure 5-3.

20. Working from the top of the A9 module, unsolder the two leads on the A9 module which are connected to the front panel PHONES jack.

21. Unsolder the leads on the A9 module which are connected to the IF Gain Control and to the AF Gain Control.

5.7.20 A9 Module Installation

Installation of the A9 module is the reverse of removal with the following notes:

1. Connect leads from front panel controls as shown in diagram in step 19 of A9 module removal.

2. Ensure ribbon leads from keypads are firmly seated in connectors A9J2 and A9J3 before installing holddown screws and hardware.

3. Tighten tuning shaft assembly retaining nut only finger tight.

CAUTION

Ensure that the nylon washer is in place between the A9 module and the tuning shaft assembly retaining nut. Absence of this washer (insulator) may cause electrical damage to the A9 module.

CAUTION

Do not overtighten the tuning shaft assembly. Use finger pressure only. Overtightening may cause damage to A9 module, and will cause abnormal tightness of the manual tuning shaft.

5.7.21 A10 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.

2. Remove the receiver top cover as directed in Paragraph 5.7.2.

3. Loosen (counterclockwise) the four (4) ¼ turn fasteners on the A10 module cover.

4. Lift out the A10 module cover.

5. Remove the Bandwidth Filter cover as directed in Paragraph 5.7.25.1.

6. Disengage the locking clips (2 each) on connectors A10J2 and A10J3 located on the outside of the A10 module.

7. Carefully unplug the connectors from A10J2 and A10J3.

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8. Loosen and remove the five (5) screws and hardware (located on the outside of the rear panel) which hold the back panel of the A10 module to the rear panel of the Receiver. Loosen the four captive screws at the base of the A10 module.

9. Grasping the sides of the A10 module, slide the module away from the rear panel while lifting the end of the A10 module nearest the Bandwidth Filters and lift out the A10 module.

NOTE

Take care not to crush the A10J2 or A10J3 connectors, the cooling fins on A10U1 or A10U2, or to snag the WP2 wire which connects to A4J1.

5.7.22 A10 Module Installation

Installation of the A10 module is the reverse of removal with the following cautions:

CAUTION

Move ribbon connectors W19P3 and W20P1 out of the way when installing the A10 module. Failure to do so may result in damage to the A4 module or the cooling fins on the rear of the A10 module.

CAUTION

When installing the A10 module cover, ensure that the lower edge of the cover clears the nylon cable clamp on the small ribbon cable joining W19P3. Failure to do so may cause damage to the cable, cable clamp, or A10 module cover.

5.7.23 Edgelight Assembly Removal and Installation

5.7.23.1 Edgelight Removal

1. Perform steps 1 through 19 of the A9 module Removal Procedure in Paragraph 5.7.19.

2. Using a nut driver, loosen and remove the three (3) nuts which hold the edgelight board to the front panel.

3. Carefully lift the edgelight assembly off of the front panel being careful to clear the three (3) mounting posts along the upper edge of the assembly.

5.7.23.2 Edgelight Installation

Installation of the Edgelight assembly is the reverse of removal.

CAUTION

Be careful when installing the edgelight assembly not to bump the edgelights. Bumping them may cause damage to the lights or printed circuit track on the edgelight assembly.

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5.7.24 Keypad Removal and Installation

5.7.24.1 Keypad Removal

1. Perform steps 1 through 19 of the A9 Module Removal procedure in Paragraph 5.7.19.
2. Perform the Edgelight Removal procedure in Paragraph 5.7.23.1.
3. Remove the five (5) nuts which hold the plastic keypad protective cover to the front panel.
4. Lift out the keypad protective cover.
5. Grasp the ribbon lead near the keypad and lift out the keypad.

5.7.24.2 Keypad Installation

Installation of the keypads is the reverse of removal.

5.7.25 IF Bandwidth Filter Removal and Installation

5.7.25.1 Bandwidth Filter Removal (Optional Plug-In Crystal Filters Only)

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the receiver top cover as directed in Paragraph 5.7.2.
3. Loosen the two (2) captive screws in the Bandwidth Filter Cover (nearest the receiver frame) which hold the cover to the A4 module.
4. Loosen and remove the one (1) non-captive screw in the Bandwidth Filter Cover (on the side opposite the two captive screws). Be careful not to lose the lockwasher and flatwasher which fit between the Bandwidth Filter cover and the A4 module.
5. Lift off the Bandwidth Filter cover.
6. Grasp the filter to be removed between thumb and forefinger. With a gentle side-to-side rocking motion, carefully work the filter out of its slot in the A4 module.
7. Repeat step 6 for each filter to be removed making note of which filter is installed in each slot.

5.7.25.2 Bandwidth Filter Installation (Optional Plug-In Crystal Filters Only)

Installation of the Bandwidth Filters is the reverse of removal with the following note:

NOTE

If the Receiver is to be operated with the ISB option, both upper and lower sideband filters must be installed in the Receiver. Additionally, the lower sideband filter must be installed in the FL1 position. If the Receiver is not to be operated with the ISB option, either a lower sideband filter or symmetrical sideband filter may be installed in the FL1

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position. If a lower sideband filter is installed, the companion upper sideband filter must also be installed in one of the remaining filter positions. If a symmetrical sideband filter is used, the Receiver will use the filter installed in the FL1 position for both sidebands by making the appropriate frequency offsets to the first and second local oscillators.

The remaining filters may be installed in any sequence in filter positions FL2 through FL7. However, in order to simplify system operation and troubleshooting, it is recommended that a format be established and used for all Receivers at a particular site. A typical format would be to insert the USB filter (if used) in position FL2 and insert filters with increasing bandwidths in filter positions 3 through 7.

Once the filter complement and arrangement has been determined, the following procedure should be used to insert the filters into the Receiver:

1. Working from the front of the Receiver, position the filter to be used for LSB operation over filter position FL1 (the filter position closest to the rear of the Receiver). Make certain that the large pins are aligned with the large sockets and the smaller pins are aligned with the smaller sockets.

2. Carefully push down on the filter to insert the pins into the sockets. Relatively light pressure is required to insert the pins into the sockets. If the filter does not easily slide into place, recheck the pin/socket alignments.

3. Insert the appropriate filters into filter positions FL2 through FL7 (as required), using the procedures described in steps 1 and 2.

4. After all filters have been inserted, visually inspect the filters to insure that they are properly seated. The bottom of the filters should be flat against the surface of the A4 board.

5. Replace the RF shield over the filters and secure the shield in place by tightening the three screws.

5.8 OPERATIONAL FAULT SYMPTOM CHART

Table 5-6 contains typical operational fault symptoms and their most probable causes. The table should be used as a guideline only, and should be supplemented with the BITE check detailed in Paragraph 5.4.2 and the Performance Tests detailed in Paragraph 5.5.

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TABLE 5-6. OPERATIONALLY BASED FAULT SYMPTOM CHART

FAULT SYMPTOMS	BOARD/MODULE PROBABLY FAULT Check Module Board According to Number Order											COMMENTS & NOTES
	A1	A2	A3	A4	A5	A6	A6A1	A7	A8	A9	A10	
Unable to energize Receiver											1	Check Power Supply
MODE LCDs blank mostly zeros in Frequency LCD						2						PC wafer in wrong position, A6A2
Unable to establish LOCAL operating condition						1				2		A6A2, A9
FAULT LED illuminated								1	2			Synthesizer failure, A7, A8, S2 switch in wrong position
BITE error code display												See BITE error code chart
Unable to exit LOCK Mode						2				1		A9, A6A2
No manual tuning										1		A9
No meter level indication in AF or RF	2			1								A4, A1
No audio output				1								A4
No audio output ISB only					1							A5
Unable to adjust Line Level Out				1								A4

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TABLE 5-6. OPERATIONALLY BASED FAULT SYMPTOM CHART (Cont.)

FAULT SYMPTOMS	BOARD/MODULE PROBABLE FAULT											COMMENTS & NOTES
	A1	A2	A3	A4	A5	A6	A6A1	A7	A8	A9	A10	
	Check Module Board According to Number Order											
No Remote Data entry/return							1					A6A1
No tone from BFO in CW mode									1			A8 - Confirm CW signal present and not in BFO CENTER
Displayed IF bandwidth does not match any installed filter				2								Check filters, A4
Unable to enter frequency from receiver front panel						3				2		Confirm Receiver not in Remote
IF output at J2 not at 455 kHz						3		2	1			A8, A7, A4
Unable to initialize BITE routine						2				1		Confirm Receiver not in Remote
Receiver does not retain frequency data after Power Interrupt						1						Check Battery

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SECTION VI
REPLACEMENT
PARTS LIST

6.1 INTRODUCTION

This section contains a complete listing of all replaceable parts contained in the RA6790/GM receiver. The parts list tables are arranged in sequence by unit designation.

Since electromechanical equipment undergoes periodic changes over time, due to factors such as operational time, environmental conditions, etc., degradation of individual subassemblies and parts occur. Replacement Parts Lists act as reference guides for users and must be consulted to identify and locate parts. To be able to identify and locate parts the user must be familiar with the unit designation method, reference designator prefixes, illustrations and schematics. The unit designation is a method of assigning reference designations (electrical symbol numbers to identify assemblies or modules, subassemblies or submodules). This method is composed of assigning a class letter such as R for resistor or C for capacitor followed by an identifying number -1, -2, -3, -4, etc.

This partial reference designation must be further identified by including a reference designator prefix, such as A1A6, which classes the item by assembly (A1) and subassembly (A6). The composite alphanumeric code then becomes the complete reference designation. For example A4C1 would be identified as the first (1) capacitor (C) of the fourth (4) assembly (A).

A detail part of subassembly A1A6 such as a resistor or capacitor would be numbered R1 or C1, resulting in a full reference designation number of A1A6C1.

If components on an assembly, module or subassembly need to be replaced, the following parts list information will provide the user with the proper ordering information. Pictures of assemblies and subassemblies along with component location diagrams are shown for ease of physically locating the desired components.

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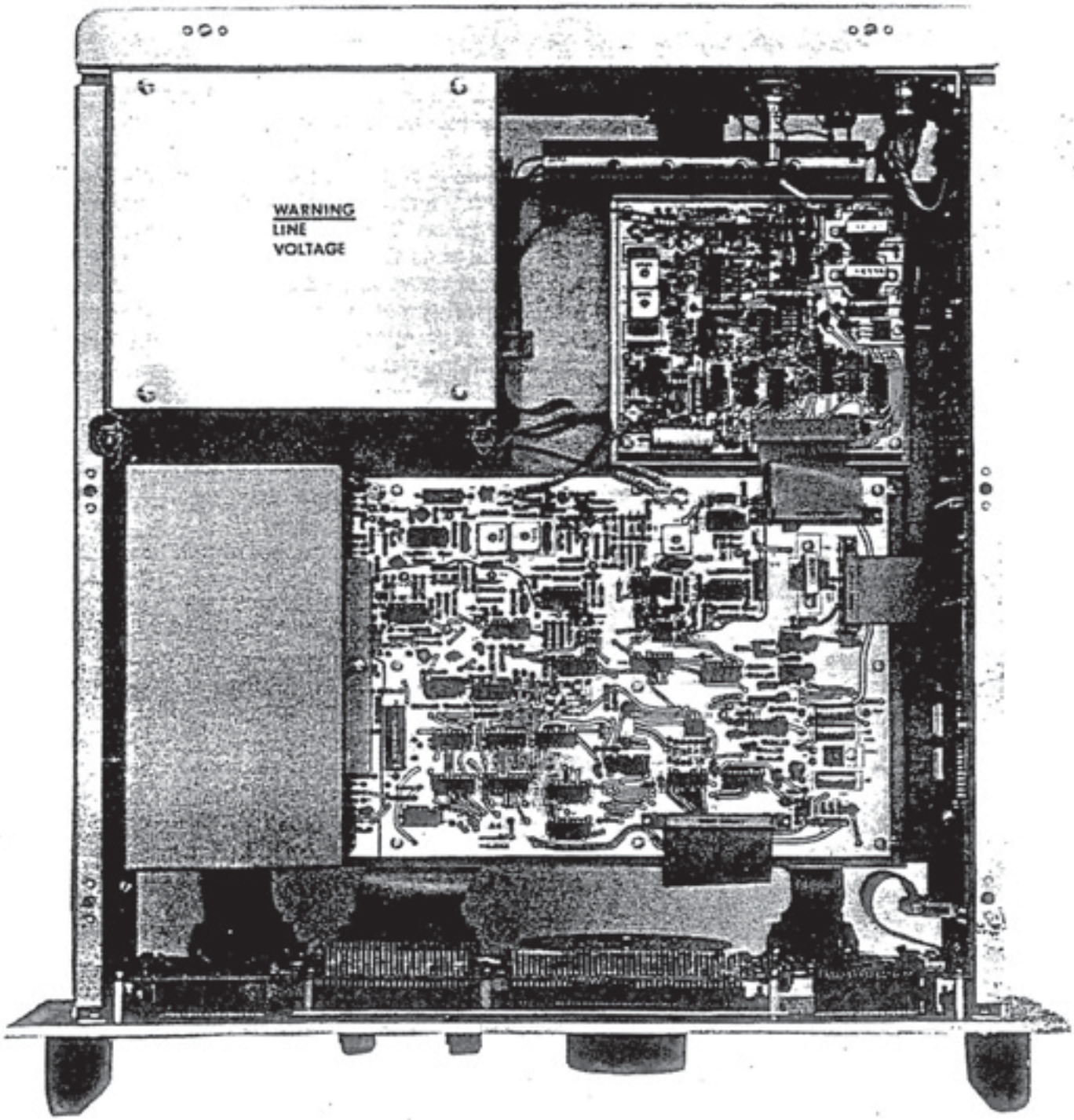

Figure 6-1. RA6790/GM Receiver, Top View

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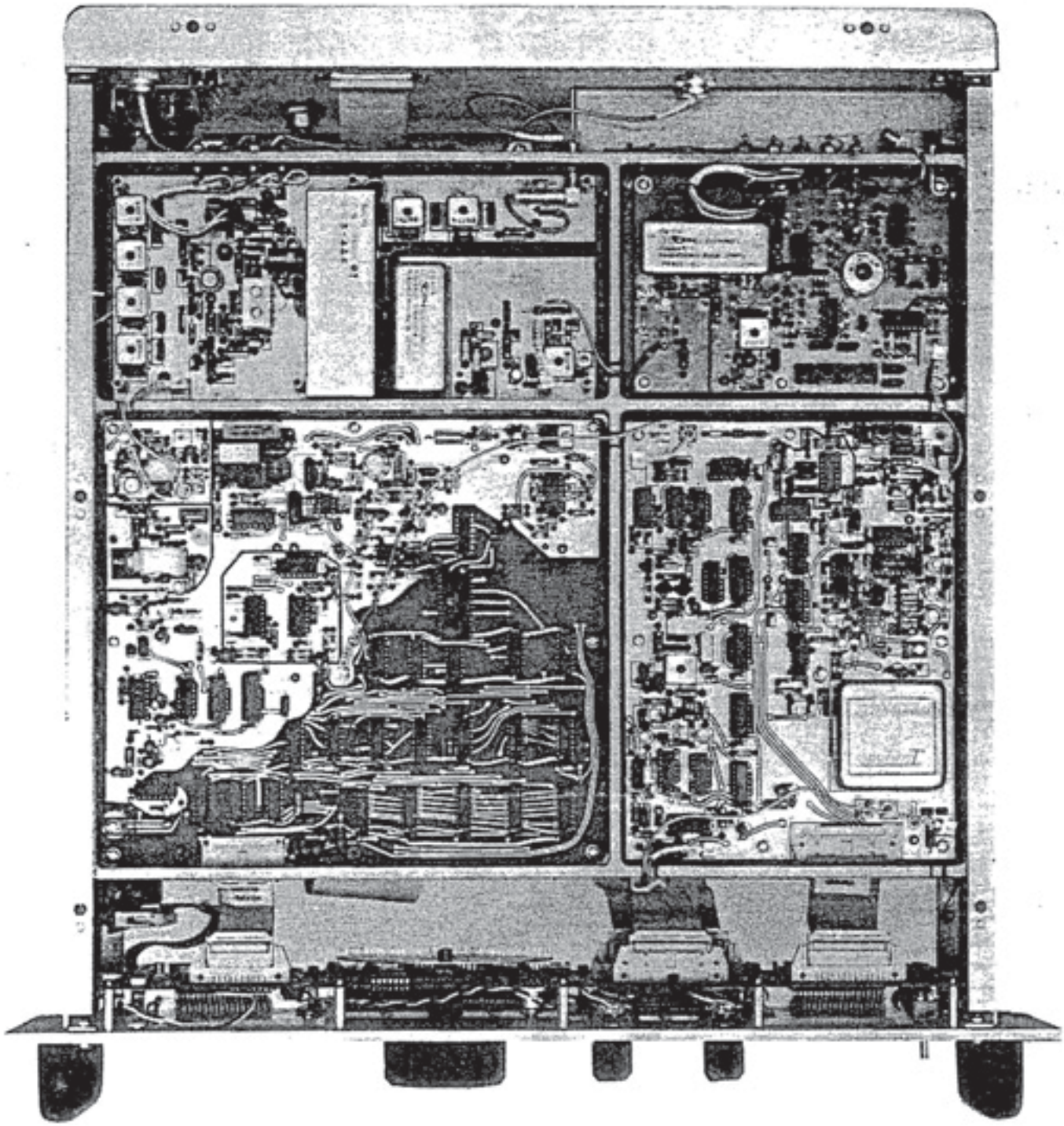

Figure 6-2. RA6790/GM Receiver, Bottom View

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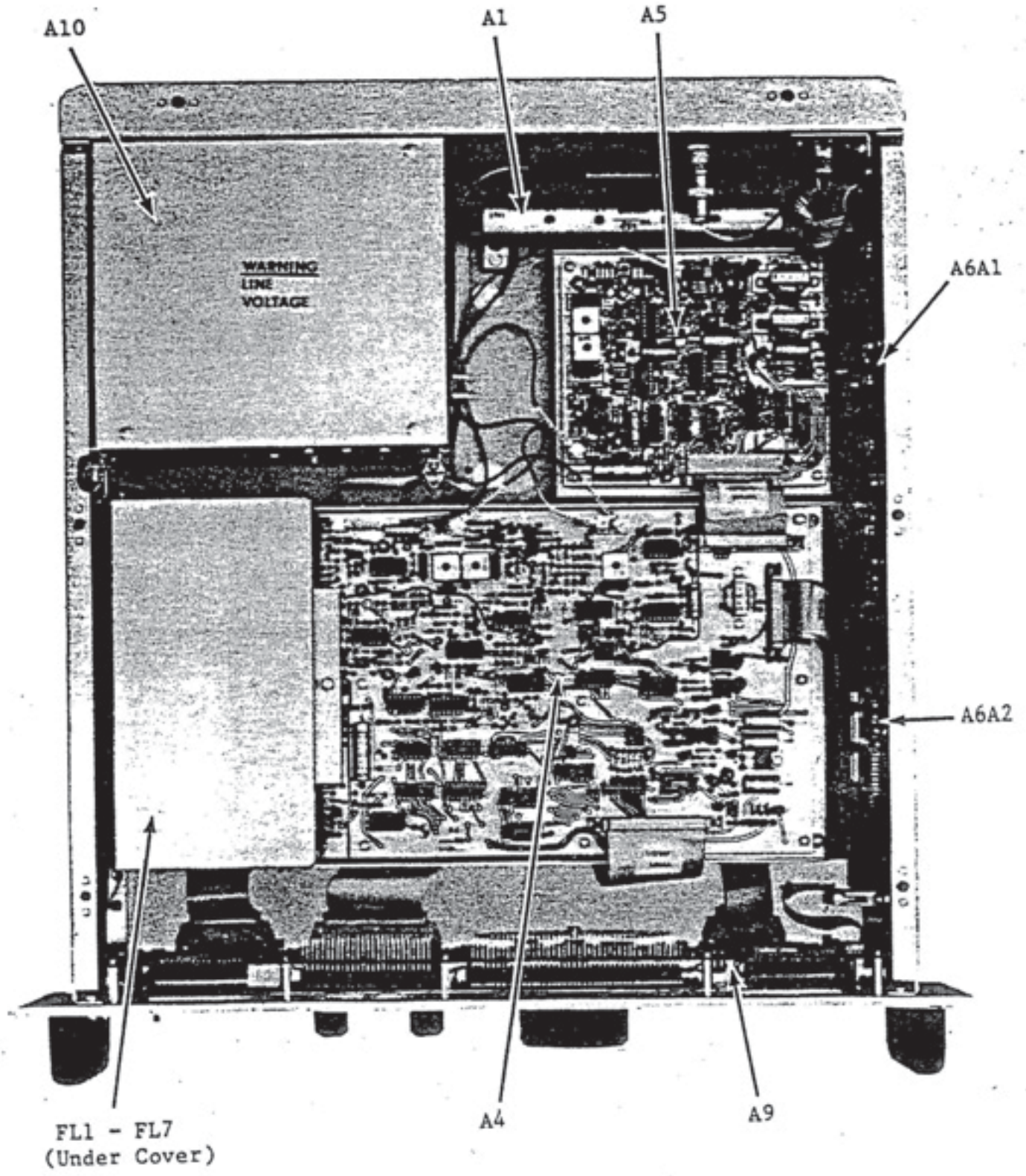

Figure 6-3. Location of Modules, Top View

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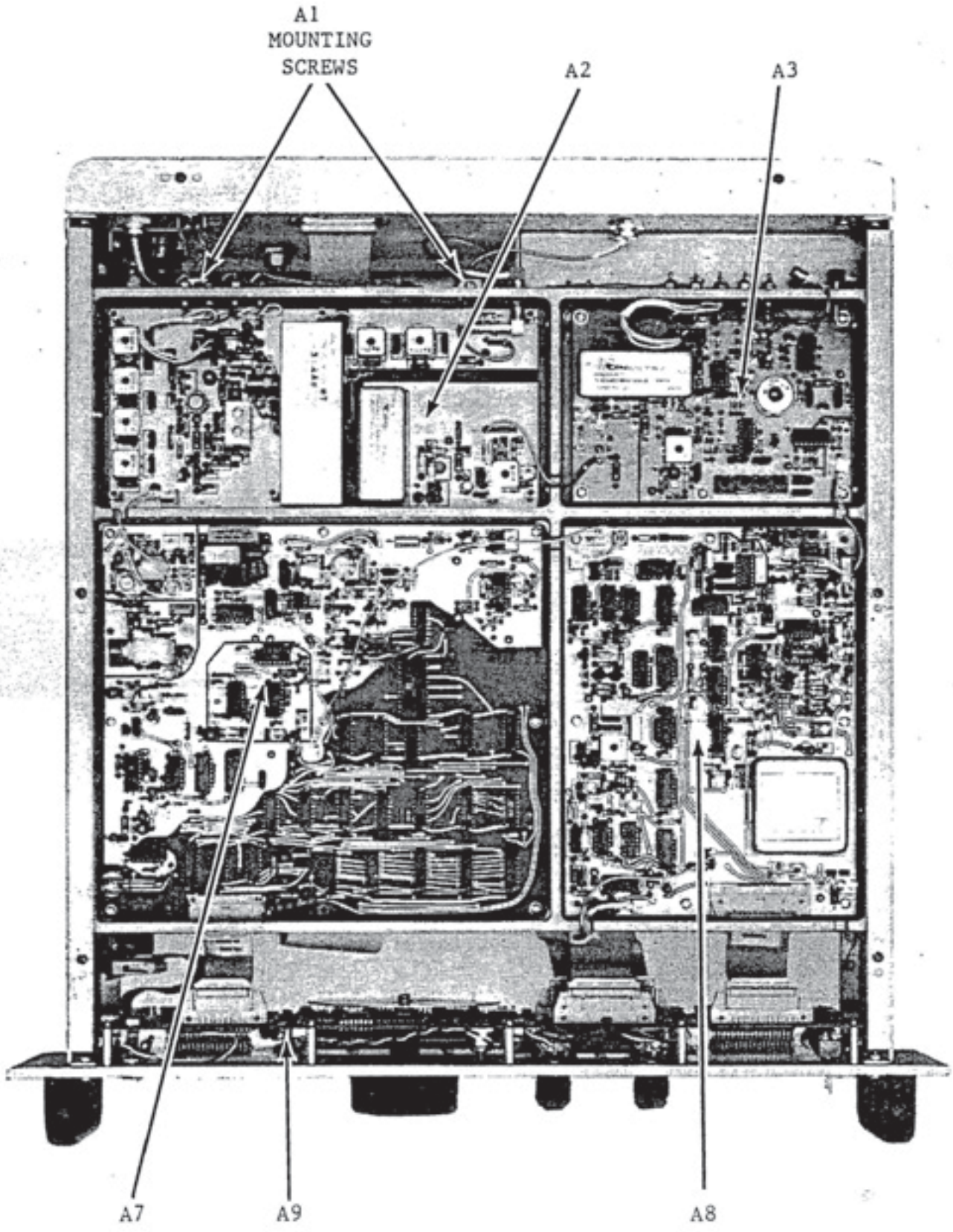

Figure 6-4. Location of Modules, Bottom View

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TABLE 6-1. PARTS LIST, RA6790/GM RECEIVER COMPONENTS

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A1	RF Low Pass Filter Module Assembly (see Table 6-2 for further breakdown)	08385	
A2	First Mixer Circuit Card Assembly (see Table 6-4 for further breakdown)	09635	
A3	Second Mixer Circuit Card Assembly (see Table 6-5 for further breakdown)	08191	
A4	Main IF/AF Circuit Card Assembly (see Table 6-6 for further breakdown	08465	
A5 (optional)	ISB Circuit Card Assembly (see Table 6-7 for further breakdown)	08390-2	
A6	Microcomputer Assembly (see Table 6-8 for further breakdown)	08397-2	
A7	First LO Synthesizer Circuit Card Assembly (see Table 6-11 for further breakdown)	09134	
A8	Second LO/BFO Synthesizer Circuit Card Assembly (see Table 6-12 for further breakdown)	09632	
-	Front Panel Assembly	08935	
A9	Receiver Control Assembly (p/o Front Panel Assembly) (see Table 6-13 for further breakdown)	08388	
A10	Power Supply Module Assembly (see Table 6-15 for further breakdown)	08389	
C1-C9	Capacitor, Feed-thru, .001 uF, ±20%	26406	BSF-1BBGP102M
C10	Capacitor, Ceramic, .01 uF, 50 WVDC ±20% (Erie)	21733	C320C103M1U1C1
J1	Connector, N-BNC, Bulkhead RF In	60063	
J2	Connector, BNC, Bulkhead IF Out (Part of Cable W12)	60046	
J3	Connector, 25-Pin, D Subminiature AF Out, (Part of Cable W16)	61248	
J4	Connector, Phone Jack	61502	JJ-034
J5, J6	Connector, SMB-SMB, Bulkhead	60057	
J7	Connector, BNC, Bulkhead Reference In/Out (Part of Cable W7)	60046	
L1	Inductor, 1000 uH, ±5%	43038	MS90539-15
R1	Potentiometer, IF Gain, 50K ohms	08552	
R2	Potentiometer, AF Gain, 25K ohms	08551	
S1	Switch, Toggle, DPDT, Miniature, Power ON (Part of Cable W20)	52424	
S2	Switch, Slide, DPDT, Reference, In/Out	52425	
S3	Switch, 16 Pushbutton, Frequency Keyboard	C09078	
S4	Switch, 16 Pushbutton, Mode Keyboard	08498-2	
W1	Cable, RF Coax	08555-1	
W2	Cable, RF Coax	08555-2	
W3	Cable, RF Coax	08555-3	
W4	Cable, RF Coax	08555-4	
W5	Not used		
W6	Cable, RF Coax	08555-5	
W7	Cable, RF Coax, Ref In/Out	08556-1	
W8, W9	Not used		

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TABLE 6-1. PARTS LIST, RA6790/GM RECEIVER COMPONENTS (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
W10	Cable, RF Coax	08555-6	
W11	Cable, RF Coax	08555-7	
W12	Cable, RF Coax, Main IF Out	08556-2	
W13	Cable, Control	08376	
W14	Cable, Control	08558	
W15	Cable, Control	08563	
W16	Cable, AF output	08568	
W17	Not Used		
W18	Cable, Power Input	57035	
W19	Cable, DC Power	08569	
W20	Cable, AC Line Switching	08570	
W21	Cable, DC Supply, A2	08561	
W22	Cable, DC Supply, A3	08560	
-	Filter, Mech, Symmetrical, 0.3 kHz	07883-1	
-	Filter, Mech, Symmetrical, 1.0 kHz	07883-2	
-	Filter, Mech, Symmetrical, 3.2 kHz	07883-3	
-	Filter, Mech, Symmetrical, 6.0 kHz	07883-4	
-	Filter, Mech, USB, 450 Hz to 3000 Hz	07883-5	
-	Filter, Mech, LSB, 450 Hz to 3000 Hz	07883-6	
A4C1,A4C2	Capacitor, Mica, 270 F, ±2%	22103	
A4C3	Capacitor, Mica, 270 pF, ±2%	22118	
A4C4	Capacitor, Mica, 110 pF, ±2%	22139	
A4C5	Capacitor, Mica, 360 pF, ±2%	22173	
A4C6,A4C12	Capacitor, Mica, 750 pF, ±2%	22172	
A4C7, A4C8	Capacitor, Mica, 240 pF, ±2%	22170	
A4C9	Capacitor, Mica, 150 pF, ±2%	22101	
A4C10	Capacitor, Mica, 82 pF, ±2%	22108	
A4C11	Capacitor, Mica, 330 pF, ±2%	22117	
A4C109	Capacitor, optional depending upon		
A4C110	FL7 filter selection; not used when link installed		
	Diffuser, Light	09500	
	LCD/LED Board Assembly	A09501	
	See Table 6-14 for further breakdown		

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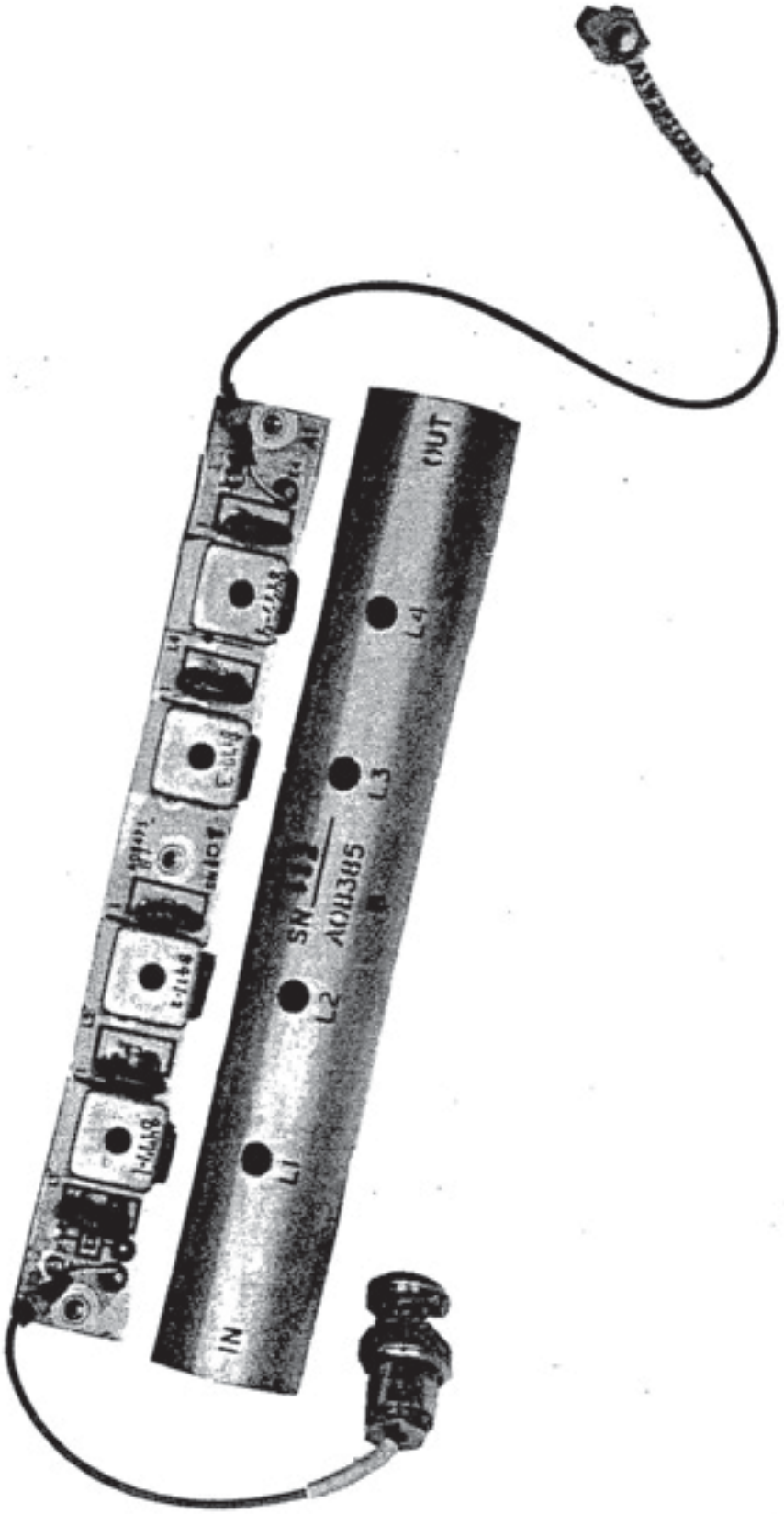

Figure 6-5. Low Pass Filter Assembly, A1

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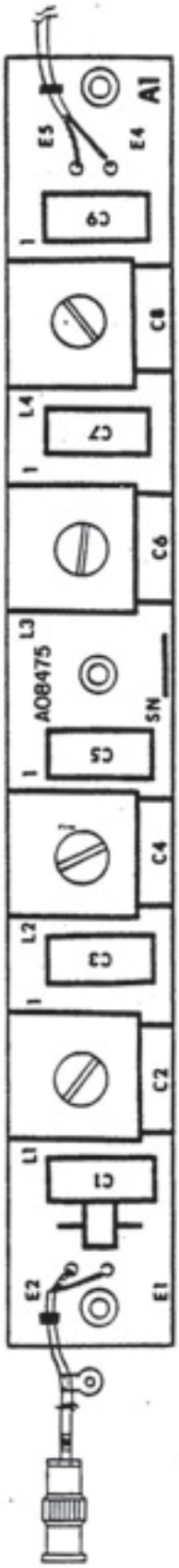

Figure 6-6. Component Location Diagram, A1

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TABLE 6-2. PARTS LIST, RF LOW PASS FILTER MODULE ASSEMBLY, A1

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A1A1	RF Low Pass Filter Circuit Card Assembly (see Table 6-3 for further breakdown)	08475	

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TABLE 6-3. PARTS LIST, RF LOW PASS FILTER CIRCUIT CARD ASSEMBLY, A1A1

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
C1, C5	Capacitor, Mica, 110 pF, 500 WVDC, ±2%	22139	CMR05F111G0DR
C2	Capacitor, 10 pF, 500 WVDC, ±5%	22161	CMR05C100D0DR
C3	Capacitor, Mica, 150 pf, 500 WVDC, ±2%	22101	CMR05F151G0DR
C4	Capacitor, Mica, 75 pF, 500 WVDC, ±5%	22020	CMR05E750G0DR
C6	Capacitor, Mica, 91 pF, 500 WVDC, ±2%	22123	CMR05F910G0DR
C7	Capacitor, Mica, 120 pF, 500 WVDC, ±2%	22113	CMR05F121G0DR
C8	Capacitor, Mica, 43 pF, 500 WVDC, ±2%	22137	CMR05E430G0DR
C9	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	CMR05E820G0DR
L1	Coil, RF Variable	08477-1	
L2	Coil, RF Variable	08477-2	
L3	Coil, RF Variable	08477-3	
L4	Coil, RF Variable	08477-4	
W1	Cable Assembly	08480	
W2	Cable Assembly	08479-4	

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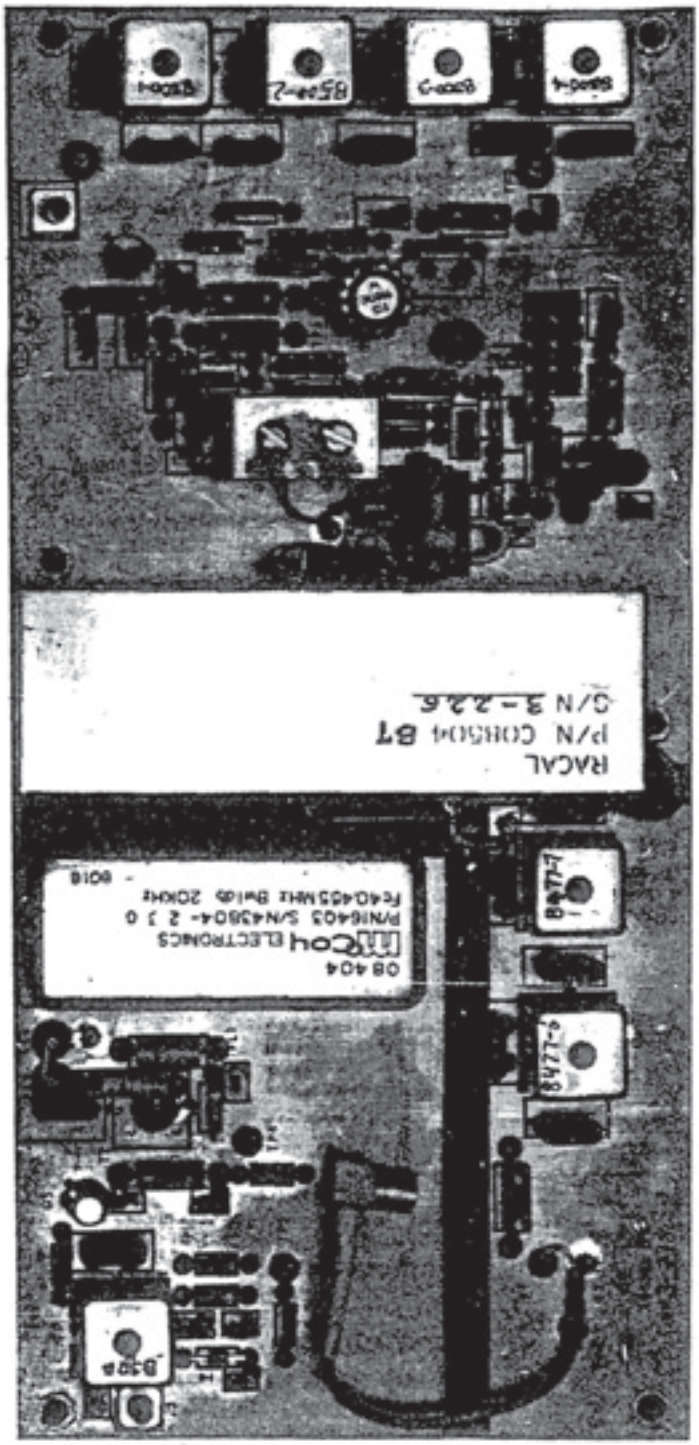

Figure 6-7. First Mixer Assembly, A2

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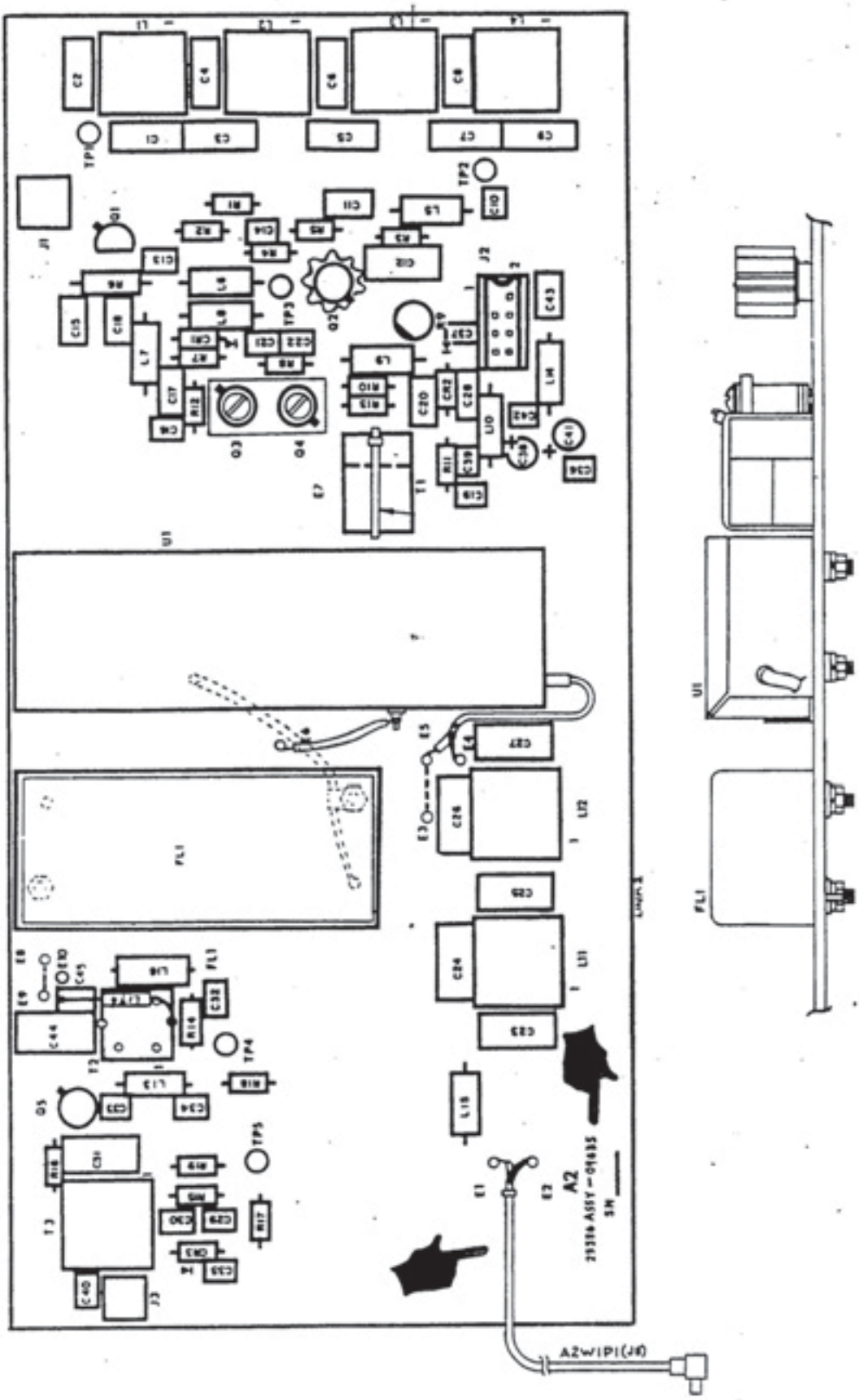

Figure 6-8. Component Location, A2

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TABLE 6-4. PARTS LIST, FIRST MIXER CIRCUIT CARD ASSEMBLY, A2

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A2	First Mixer, Circuit Card Assembly	09635	
C1, C3	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	CMR05E820G0DR
C2, C7	Capacitor, Mica, 150 pF, 500 WVDC, ±2%	22101	CMR05F151G0DR
C4	Capacitor, Mica, 18 pF, 500 WVDC, ±2%	22129	CM05CD180G0DR
C5	Capacitor, Mica, 270 pF, 500 WVDC, ±2%	22103	CMR05F271G0DR
C6	Capacitor, Mica, 10 pF, 500 WVDC, ±½ pF	22161	CMR05C100G0DR
C8	Capacitor, Mica, 30 pF, 500 WVDC, ±2%	22160	CMR05E300G0DR
C9	Capacitor, Mica, 240 pF, ±2%	22170	
C10, C13, C14, C21, C22, C29, C34, C36, C37, C39, C42	Capacitor, Ceramic, 0.02 uF, 50 WVDC, ±20%	21733	C320C103M1U1C1
C11, C15, C18, C28, C43	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	MS39014/01-1593
C12, C45	Capacitor, Not Used		
C16, C19, C30, C32, C33, C35, C40, C45	Capacitor, Ceramic, 0.001 uF, 18 WVDC, ±20% (Centralab)	21756	CY15C102M
C17, C20	Capacitor, Ceramic, 1 uF, 500 WVDC, ±20%	21748	MS39014/02-1419
C23, C25	Capacitor, Mica, 100 pF, 500 WVDC, ±2%	22109	CM05ED101J03
C24	Capacitor, Mica, 91 pF, 500 WVDC, ±2%	22123	CMR05F910G0DR
C26	Capacitor, Mica, 43 pF, 500 WVDC, ±2%	22137	CMR05E430G0DR
C27	Capacitor, Mica, 68 uF, 500 WVDC, ±2%	22107	CMR05E680G0DR
C31	Capacitor, Mica, 33 pF, 500 WVDC, ±2%	22106	CMR05E330G0DR
C38, C41	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20% (Union Carbide)	25062-156	T362B156K1020A8
C44	Capacitor, Mica, 27 pF, 500 WVDC, ±2%	22119	CMR05E270G0DR
CR1, CR2	Diode, Silicon	35514	1N916B
CR3	Diode, Pin (Motorola)	35557	KS8379
FL1	Filter, 40.455 MHz	08404	
J1, J3	Connector, SMB	60044	051-351-0000-220
J2	Connector, Control	08499-4	
L1	Coil Assembly, RF, Variable	08500-1	
L2	Coil Assembly, RF, Variable	08500-2	
L3	Coil Assembly, RF, Variable	08500-3	
L4	Coil Assembly, RF, Variable	08500-4	
L5, L7-L10	Choke, RF, 10 uH, ±10%	43029	MS14046-4
L6	Choke, RF, 2.2 uH, ±10%	43025	MS18130-12
L11	Coil Assembly, RF, Variable	08477-6	
L12	Coil Assembly, RF, Variable	08477-7	
L13, L14	Choke, RF, 15 uH, ±10%	43030	MS14046-6
L15	Choke, RF, 0.27 uH, ±10%	43051	MS75087-6
L16, L17	Choke, RF, 0.56 uH, ±10%	43052	MS18130-5
Q1	Transistor, Silicon, PNP (Motorola)	31508	2N4126
Q2, Q4	Transistor, Silicon, High Power, NPN	32046	2N3866

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TABLE 6-4. PARTS LIST, FIRST MIXER CIRCUIT CARD ASSEMBLY, A2 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
Q3	Transistor, Silcon, High Power, PNP (Motorola)	32027	2N5160
Q5	Transistor, Field Effect (National)	32507	U310
R1, R5, R17	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R2	Resistor, Film, 5.6K, ±2%, 1/4W	12161-562	RLR07C562GR
R3	Resistor, Film, 47 ohms, ±2%, 1/4W	12161-470	RLR07C470GR
R4	Resistor, Film, 2.2K, ±2%, 1/4W	12161-222	RLR07C222GR
R6	Resistor, Composition, 15 ohms, ±5%, 1/2W	10919	RCR20G150JS
R7, R11, R14, R15	Resistor, Film, 220 ohms, ±2%, 1/4W	12161-221	RLR07C221GR
R8, R10	Resistor, Film, 1.2K, ±2%, 1/4W	12161-122	RLR07C122GR
R9	Resistor, Trimmer, 5K, ±10%	16090-502	RJ50FP502
R12, R13, R16	Resistor, Film, 10 ohms, ±2%, 1/4W	12161-100	RLR07C100GR
R18	Resistor, Film, 100 ohms, ±2%, 1/4W	12161-101	RLR07C101GR
R19	Resistor, Film, 10K, ±2%, 1/4W	12161-103	RLR07C103GR
T1	Transformer, RF, Wideband	08501	
T2	Transformer, Not used		
T3	Transformer, RF, Variable	08503	
U1	Assembly, Mixer Box	08504	
W1	Mixer Box Assembly	A08504	
-	Cable, RF Coax	B08479-1	69011-1058
-	Pad, Transistor, Q2, Q3, Q4 (Garlock)	70750	7717-N WHT
-	Pad, Transistor, Q5 (Thermalloy)	70752	2257R
-	Heat Sink, Q2	70801	J25-1104
-	Heat Sink, Q3, Q4 (Jermyn)	70784	
	Plate, Heat Sink, Q3, Q4	B09226	

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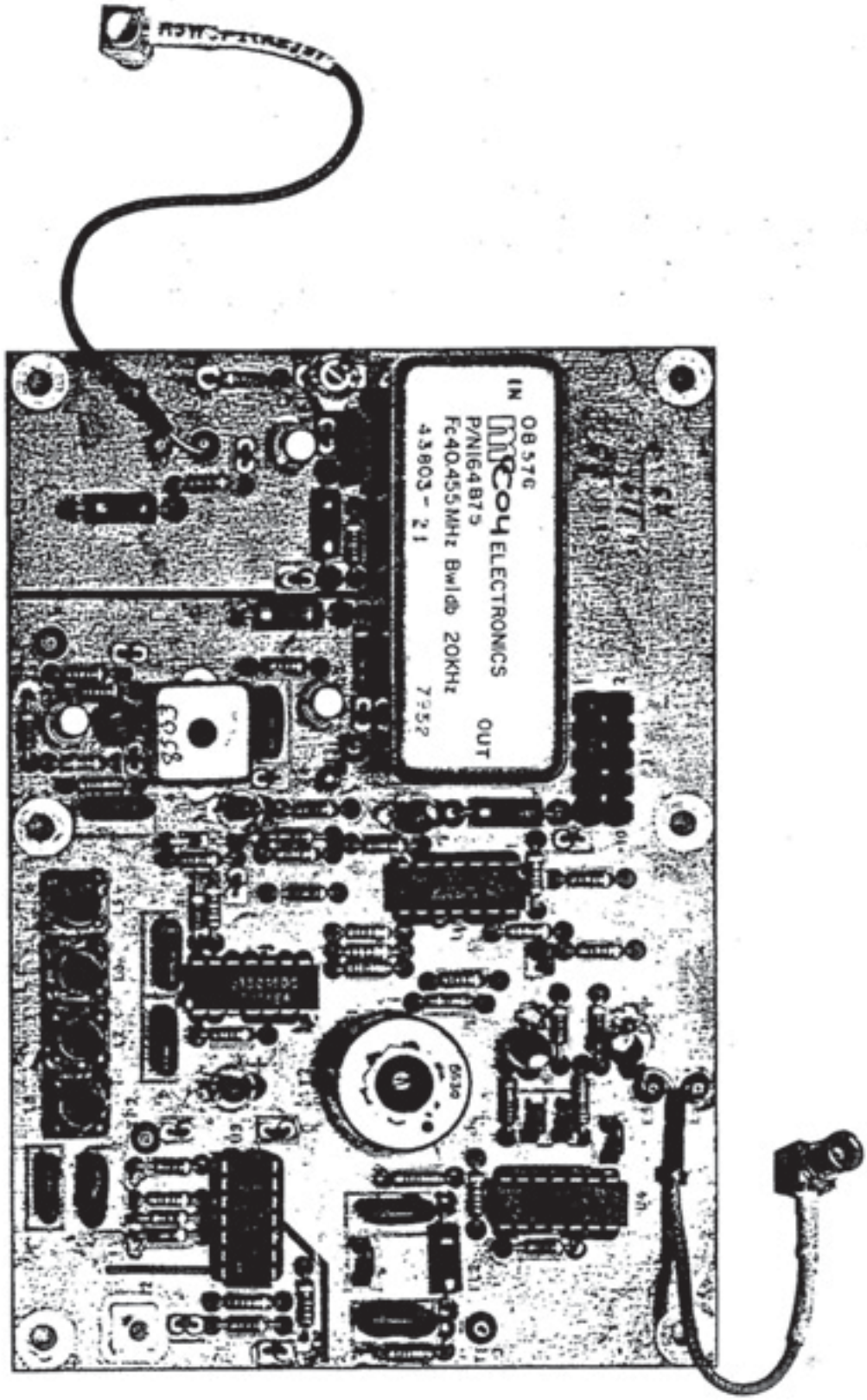

Figure 6-9. Second Mixer Assembly, A3

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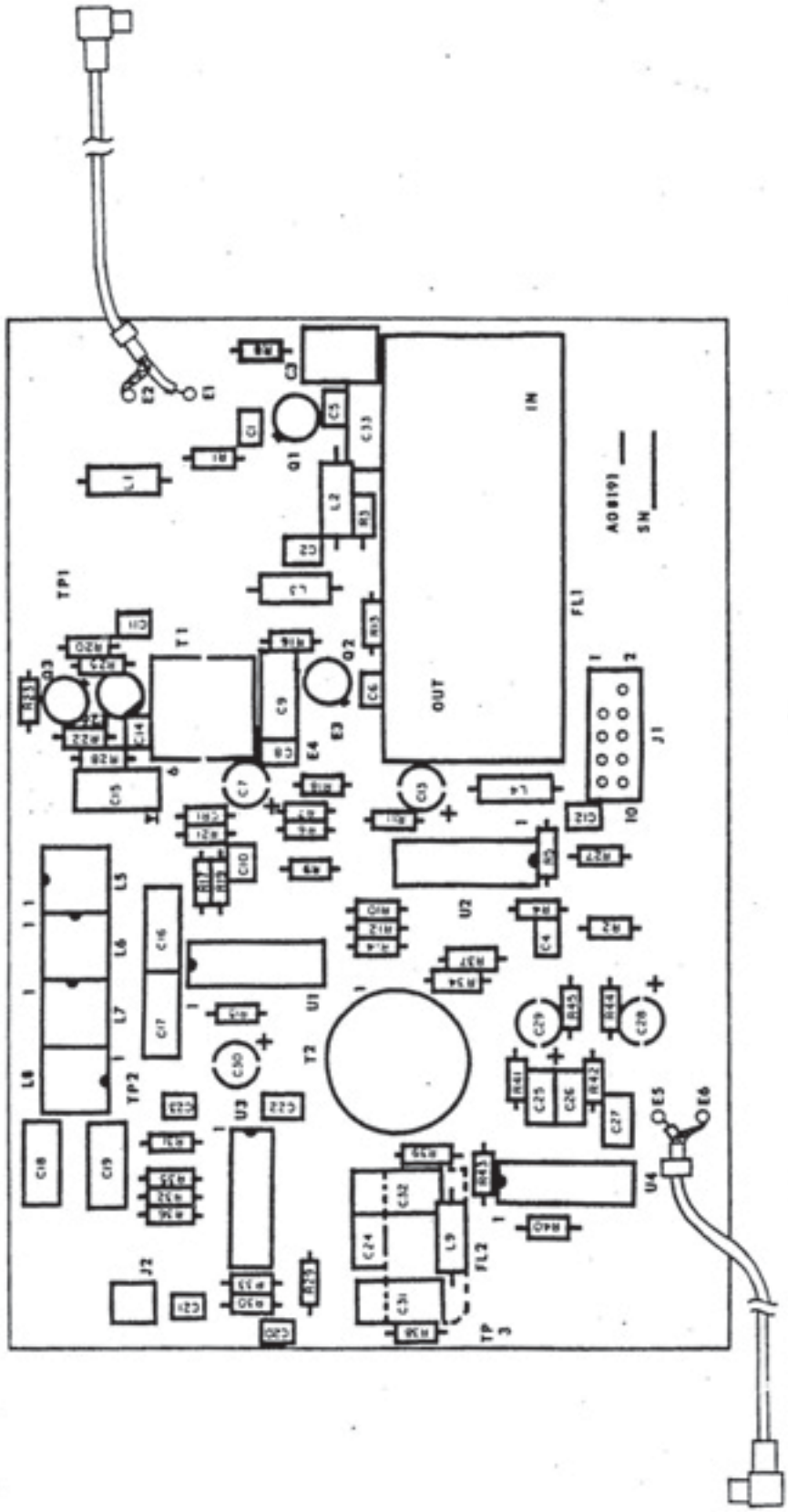

Figure 6-10. Component Location Diagram, A3

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TABLE 6-5. PARTS LIST, SECOND MIXER CIRCUIT CARD ASSEMBLY, A3

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A3	Second Mixer, Circuit Card Assembly	08191	
C1, C2, C5, C6, C8, C10, C11, C12, C14, C20, C21, C22, C23	Capacitor, Ceramic, 1000 pF, 500 WVDC, ±20% (Centralab)	21756	CY15C102M
C3	Capacitor, Variable, 5-50 pF (Johanson)	28037	9311
C4	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20% (Union Carbide)	21733	C320C103M1U1C1
C7, C30	Capacitor, Tantalum, 1 uF, 35 WVDC, ±20% (Union Carbide)	25060-105	T362A105M035AS
C9	Capacitor, Mica, 33 pF, 50 WVDC, ±2%	22106	CMR05E330G0DR
C13, C28, C29	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20%	25062-156	T362B156K020AS
C15, C16, C17	Capacitor, Mica, 68 pF, 500 WVDC, ±2%	22107	CMR05E680G0DR
C18	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	CMR05E820G0DR
C19	Capacitor, Mica, 330 pF, 500 WVDC, ±2%	22117	CMR05F331G0DR
C24 thru C27	Capacitor, Ceramic, 0.1 uF, 500 WVDC, ±20%	21732	M39014/01-1593
C31, C32	Capacitor, Mica, 22 pF, 500 WVDC, ±2%	22171	CM05ED220D03
C33	Capacitor, Mica, 15 pF, 500 WVDC, ±2%	22116	CMR05C150G0DR
CR1	Diode, Pin (Motorola)	35557	KS8379
FL1	Filter, 40.455 MHz	08576	
J1	Connector, RF In	08499-5	
J2	Connector, RF, SMB (Sealectro)	60044	051-851-0000-220
L1, L3, L9	Choke, RF, 15 uH, ±10%	43030	MS14046-6
L2	Choke, RF, 0.56 uH	43052	MS18130-5
L4	Choke, RF, 100 uH, ±5%	43033	MS90538-12

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TABLE 6-5. PARTS LIST, SECOND MIXER CIRCUIT CARD ASSEMBLY, A3 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
L5 thru L8	Coil, RF, Variable	08522	
Q1, Q2	Transistor, Field Effect (National)	32507	U310
Q3	Transistor, NPN	31500	2N918
R1, R10, R13, R18	Resistor, Film, 220 ohms, ±2%, 1/4W	12161-221	RLR07C221GR
R2, R3, R20, R21, R27, R35	Resistor, Film, 100 ohms, ±2%, 1/4W	12161-101	RLR07C101GR
R4	Resistor, Film, 220K, ±2%, 1/4W	12161-224	RLR07C224GR
R5, R6, R11	Resistor, Film, 22K, ±2%, 1/4W	12161-223	RLR07C223GR
R7, R23	Resistor, Film, 4.7K, ±2%, 1/4W	12161-472	RLR07C472GR
R8, R12, R28	Resistor, Film, 2.2K, ±2%, 1/4W	12161-222	RLR07C222GR
R9	Resistor, Film, 100K, ±2%, 1/4W	12161-104	RLR07C104GR
R14	Resistor, Film, 27 ohms, ±2%, 1/4W	12161-270	RLR07C270GR
R15	Resistor, Film, 560 ohms, ±2%, 1/4W	12161-561	RLR07C561GR
R16, R37	Resistor, Film, 10 ohms, ±2%, 1/4W	12161-100	RLR07C100GR
R17, R36	Resistor, Film, 10K, ±2%, 1/4W	12161-103	RLR07C103GR
R19, R29, R33	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R22	Resistor, Film, 39K, ±2%	12161-393	RLR07C393GR
R24	Resistor, not used		
R25	Resistor, Film, 56 ohms, ±2%, 1/4W	12161-560	RLR07C560GR
R26	Resistor, Trimmer, 500 ohms, ±20%	16090-501	RJ50FP501
R30, R31, R32, R40, R44, R45	Resistor, Film, 47 ohms, ±2%, 1/4W	12161-470	RLR07C470GR
R34	Resistor, Film, 39 ohms, ±2%, 1/4W	12161-390	RLR07C390GR
R38, R39	Resistor, Film, 1.2K, ±2%, 1/4W	12161-122	RLR07C122GR

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TABLE 6-5. PARTS LIST, SECOND MIXER CIRCUIT CARD ASSEMBLY, A3 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R41, R42	Resistor, Film, 330 ohms, ±2%, 1/4	12161-331	RLR07C331GR
R43	Resistor, Film, 1.5K, ±2%, 1/4W	12161-152	RLR07C152GR
T1	Transformer, RF, Variable	08503	
T2	Transformer Assembly	08530	
U1	IC, Transistor Array (RCA)	36785	CA3046F
U2	IC, Quad Op-Amp (RCA)	36784	CA324E
U3	IC, Second Mixer (Motorola)	36748	MC1496L
U4	IC, Op-Amp (Motorola)	36747	MC1733L
W1	Cable, 40.455 MHz Input	08479-2	
W2	Cable, 455 kHz Output	08479-3	
-	Pad, Transistor, Q1, Q2, Q3 (Thermalloy)	70752	7717-7N WHT

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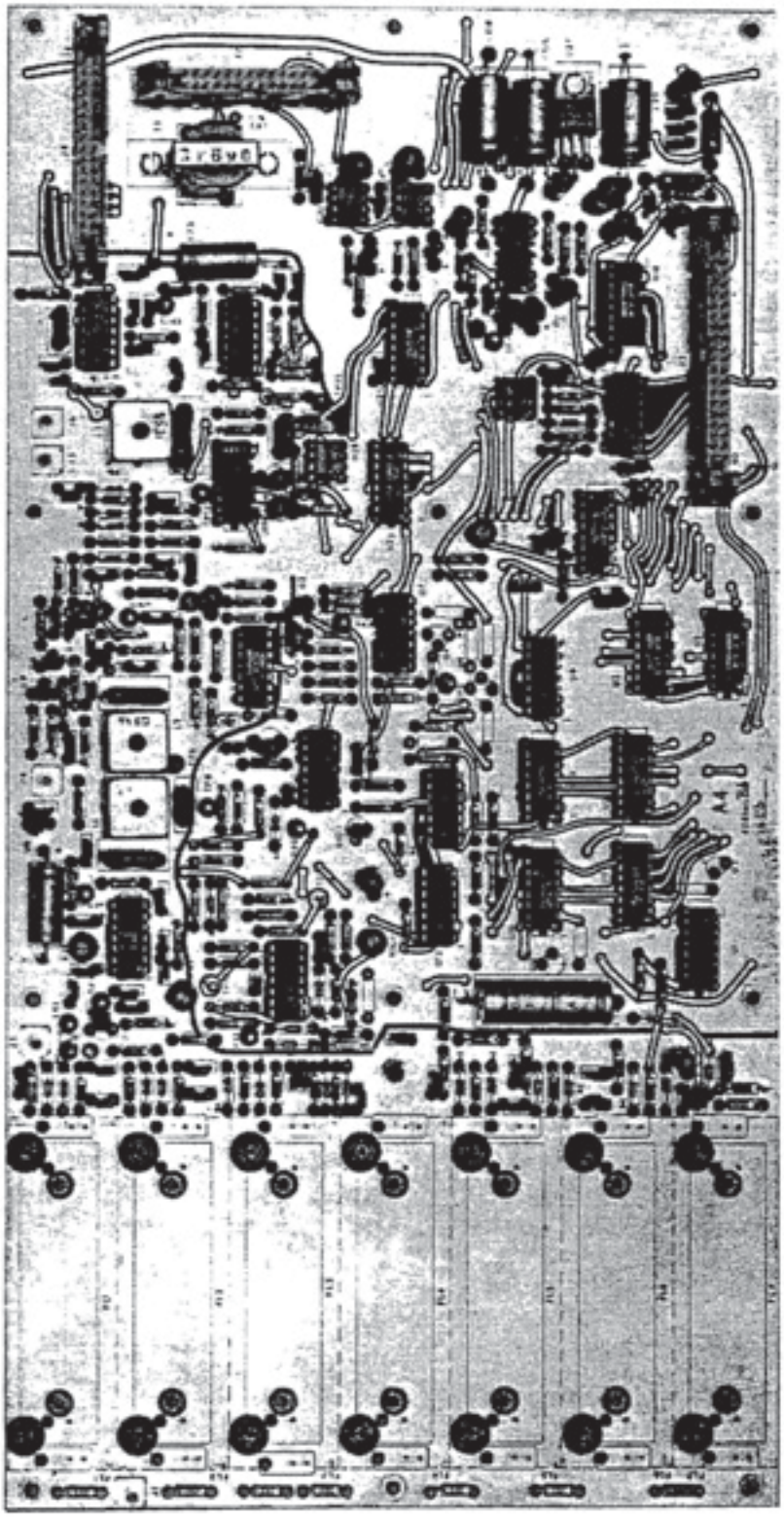

Figure 6-11. Main IF/AF Assembly, A4

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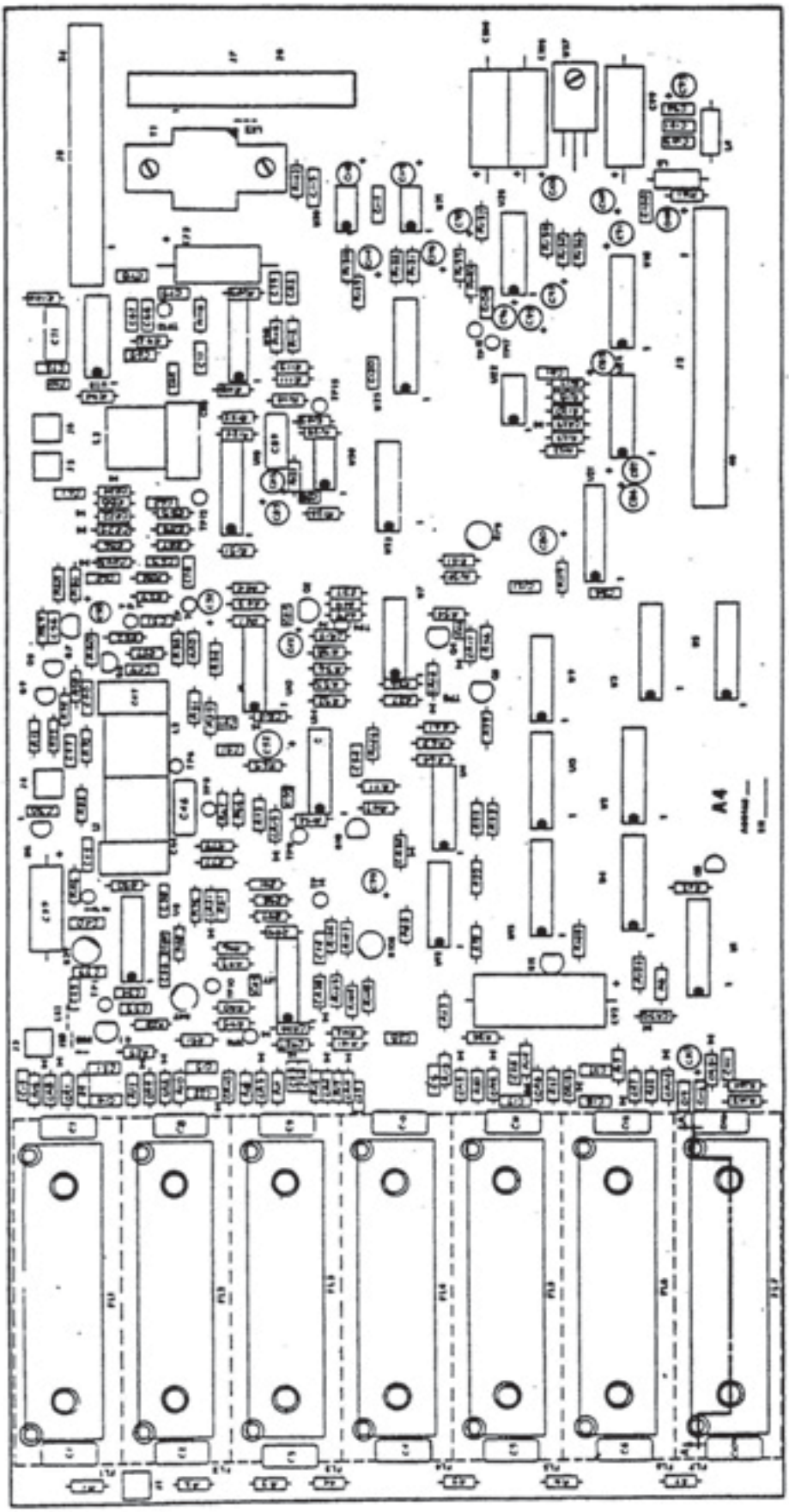

Figure 6-12. Component Location, A4

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TABLE 6-6. MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A4	Main IF/AF Circuit Card	08465	
C1 thru C12, C109, C110	Capacitor, used with Mechanical Filters 07883-1 to 07883-6. (See Table 6-1.)		
C13 thru C19, C21 thru C31, C33, C34, C36, C38, C39, C40, C45, C49, C50, C54, C56, C57, C60 thru C67, C72, C75 thru C79, C81 C82, C94, C100, C101, C103, C104, C111, C112, C120, C121	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	M39014/01-1593
C20, C32, C52, C58, C80, C93, C102, C113	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20% (Union Carbide)	25062-156	T362B156K020AS
C35, C73	Capacitor, Electrolytic, 100 uF, 25 WVDC, -10 +50% (Electra)	24066	ET101X025A5
C37	Capacitor, Ceramic, 1000 pF, 50 WVDC, ±20% (Union Carbide)	21756	8101-050-651-102M
C41	Capacitor, Ceramic, 0.022 uF, 50 WVDC, ±20% (Union Carbide)	21762	8121
C42, C59, C83, C85, C91, C95 thru C98, C106	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C43, C51, C53, C69, C70	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20%	21733	8121-050-651-103M
C44, C47	Capacitor, Mica, 1500 pF, 500 WVDC, ±2%	22174	CMR06F152GODR

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TABLE 6-6. MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
C46	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	CMR05E820GODR
C48, C55, C90	Capacitor, not used		
C68	Capacitor, Mica, 3300 pF, 500 WVDC, ±2%	22145	CMR06F332GODR
C71	Capacitor, Mica, 100 pF, 500 WVDC, ±2%	22109	CM05D101JGODR
C74	Capacitor, Ceramic, 1 uF, 50 WVDC, ±20%	21748	8131-U50-652-105M
C84	Capacitor, Ceramic, 10 pF, ±5%	21347	831-000-COH0-100C
C86, C87, C114, C116	Capacitor, Tantalum, 1.0 uF, 35 WVDC, ±10% (Union Carbide)	25060-105	T362A105M035AS
C88	Capacitor, Ceramic, 1500 pF, 100 WVDC, ±10% (Union Carbide)	21735	C320C152K2R5C1
C89	Capacitor, Ceramic, 820 pF, 300 WVDC, ±5% (Cornell)	22156	CD15FC821G03
C92	Capacitor, Electrolytic, 470 uF, 25 WVDC, (Electra)	24058	ET471X025A01
C99, C105, C108	Capacitor, Electrolytic, 220 uF, 16 WVDC, -10 +50% (Electra)	24067	3071FE221T016SF
C107, C118, C119	Capacitor, Tantalum, 68 uF, 15 WVDC, ±20% (Union Carbide)	25063-686	T362C686M015AS
C109, C110	Capacitor, see Table 6-1.		
C115, C117	Capacitor, Ceramic, 390 pF, 500 WVDC, ±20% (Erie)	21765	831-000-X5F0391K
CR1 thru CR16, CR18 thru CR31	Diode, Silicon	35514	1N916B
CR17	Diode, not used		
J1, J3 thru J6	Connector, RF (Sealectro)	60044	051-851-0000-220
J2	Connector, Ribbon, 40-way (3M)	61271	3432-2003
J7	Connector, Ribbon, 26-way (3M)	61269	3429-2003
J8	Connector, Ribbon, 34-way (3M)	61270	3431-2003

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TABLE 6-6. MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
L1, L2	Coil Assembly, RF	08485	
L3	Coil Assembly, RF	08531	
L4, L5	Choke, 100 uH, ±5%	43033	MS90538-12
Q1, Q2, Q6 thru Q10	Transistor, NPN, High Power (Motorola)	32021	2N5089
Q3, Q4, Q5, Q11	Transistor, not used		
R1 thru R7, R50, R92, R126, R136, R137	Resistor, Film, 4.7K, ±2%, 1/4W	12161-472	RLR07C472GR
R8, R29, R46, R80 R82, R115	Resistor, Film, 47 ohms, ±2%, 1/4W	12161-470	RLR07C470GR
R9 thru R15, R23, R28, R55, R62, R66, R68, R70, R72, R77, R78, R79, R85, R87, R102, R144, R145	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R16 thru R22, R24, R33, R36, R40, R53, R57, R58, R71, R86, R88, R89, R130, R132, R135	Resistor, Film, 10K, ±2%, 1/4W	23262-103	RLR07C103GR
R25, R60, R141	Resistor, Film, 100 ohms, ±2%, 1/4W	12161-101	RLR07C101GR
R26, R30, R49, R61, R73, R83, R91, R124, R147	Resistor, Film, 22K, ±2%, 1/4W	12161-223	RLR07C223GR

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TABLE 6-6. PARTS LIST, MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R27, R44, R64, R94, R113, R143	Resistor, Film, 1.5K, ±2%, 1/4W	12161-152	RLR07C152GR
R31, R84, R109, R111, R112, R114, R116, R121	Resistor, Film, 3.3K, ±2%, 1/4W	12161-332	RLR07C332GR
R32, R38, R41, R52, R90, R93, R103	Resistor, Film, 47K, ±2%, 1/4W	12161-473	RLR07C473GR
R34, R51, R101, R128	Resistor, Film, 2.2K, ±2%, 1/4W	12161-222	RLR07C222GR
R35, R75, R110	Resistor, Film, 470 ohms, ±2%, 1/4W	12161-471	RLR07C471GR
R37, R95, R96, R117, R122, R123, R125, R139, R140, R150, R151	Resistor, Film, 100K, ±2%, 1/4W	12161-104	RLR07C104GR
R39	Resistor, Trimmer, 2K	16090-202	RJ50FP202
R42, R54, R56, R59, R63, R138, R148, R149	Resistor, not used		
R43, R48	Resistor, Film, 680 ohms, ±2%, 1/4W	12161-681	RLR07C681GR
R45	Resistor, Film, 330K, ±2%, 1/4W	12161-334	RLR07C334GR
R47	Resistor, Trimmer, 50K	16090-503	RJ50FP503
R65, R69, R97, R107, R129, R131, R134	Resistor, Film, 15K, ±2%, 1/4W	12161-153	RLR07C153GR
R67, R104	Resistor, Film, 18K, ±2%, 1/4W	12161-183	RLR07C183GR
R74, R81, R108	Resistor, Film, 6.8K, ±2%, 1/4W	12161-682	RLR07C682GR
R76, R98	Resistor, Film, 12K, ±2%, 1/4W	12161-123	RLR07C123GR

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TABLE 6-6. PARTS LIST, MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R99, R146	Resistor, Film, 27K, ±2%, 1/4W	12161-273	RLR07C273GR
R100, R133	Resistor, Film, 10 ohms, ±2%, 1/4W	12161-100	RLR07C100GR
R105	Resistor, Trimmer, 10K	16090-103	RJ50FP103
R106	Resistor, Film, 180K, ±2%, 1/4W	12161-184	RLR07C184GR
R118	Resistor, Film, 39K, ±2%, 1/4W	12161-393	RLR07C393GR
R119	Resistor, Trimmer, 5K	16090-502	RJ50FP502
R120	Resistor, Film, 68K, ±2%, 1/4W	12161-683	RLR07C683GR
R127	Resistor, Film, 8.2K, ±2%, 1/4W	12161-822	RLR07C822GR
R142	Resistor, Film, 140 ohms, ±2%, 1/4W	12138	RN55D1400F
R152	Resistor, Film, 1 Meg., ±2%, 1/4W	12161-105	RLR07C105GR
T1	Transformer Assembly	08535	
U1	IC, BCD Decoder (National)	36575	CD40N28BCN
U2, U4, U13, U15, U23	IC, Quad Latch (RCA)	36613	4042B
U3, U5, U16	IC, Level Translator (RCA)	36790	CD40109BEX
U6	IC, 12 Volt dc Regulator (National)	36760	LM78L12AWC
U7, U14, U17	IC, Operational Amplifier (RCA)	36784	CA324E
U8	IC, IF Amplifier	36541	UA757DMQB
U9	IC, Dual D Flip-flop	36588	CD4013BE
U10	IC, Transistor Array (RCA)	36785	CA3046F
U11, U12	IC, Quad Bilateral Switch (RCA)	36792	CD4066BE
U18	IC, FM Detector and Limiting Amplifier (Motorola)	36631	MC1357L
U19	IC, Multiplexer/Demultiplexer (RCA)	36801	CD4053BEX
U20	IC, Product Detector (Motorola)	36748	MC1496L
U21	IC, Eight Bit Buffer, Multiplying (Analog Devices)	36803	AD7524JN

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TABLE 6-6. PARTS LIST, MAIN IF/AF CIRCUIT CARD ASSEMBLY, A4 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
U22, U28	IC, Dual Operational Amplfier (RCA)	36673	CA1458E
U24	IC, Quad Voltage Comparator	36693	LM339
U25	IC, 4x4 Crosspoint Switch (RCA)	36802	CD22100EX
U26	IC, Audio Amplifier, 2 Watt (National)	36777	LM377N
U27	IC, Voltage Regulator, +15 Volts	36708	M38510/10708BEA
U29	IC, not used		
U30, U31	IC, Electronic Attemuator (Motorola)	36763	MC3340L

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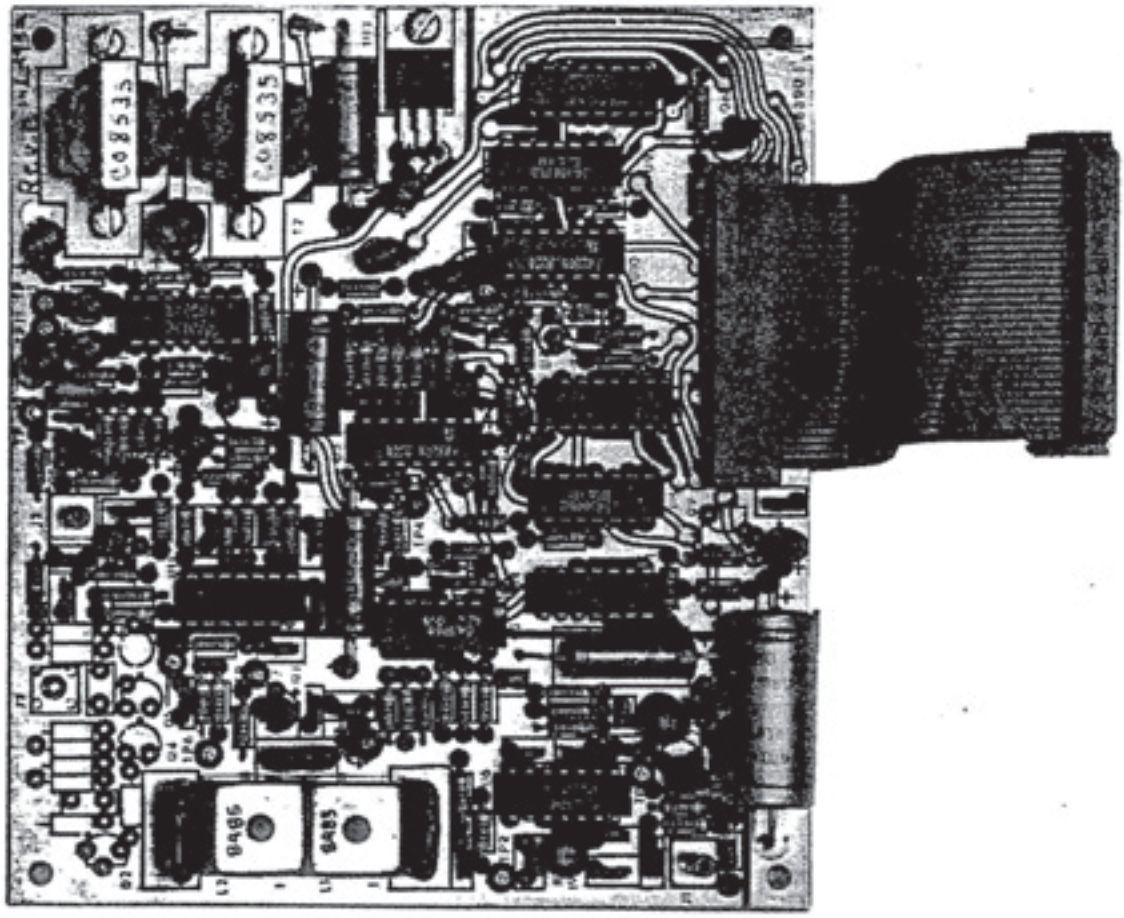

Figure 6-13. ISB Assembly, A5 (Optional)

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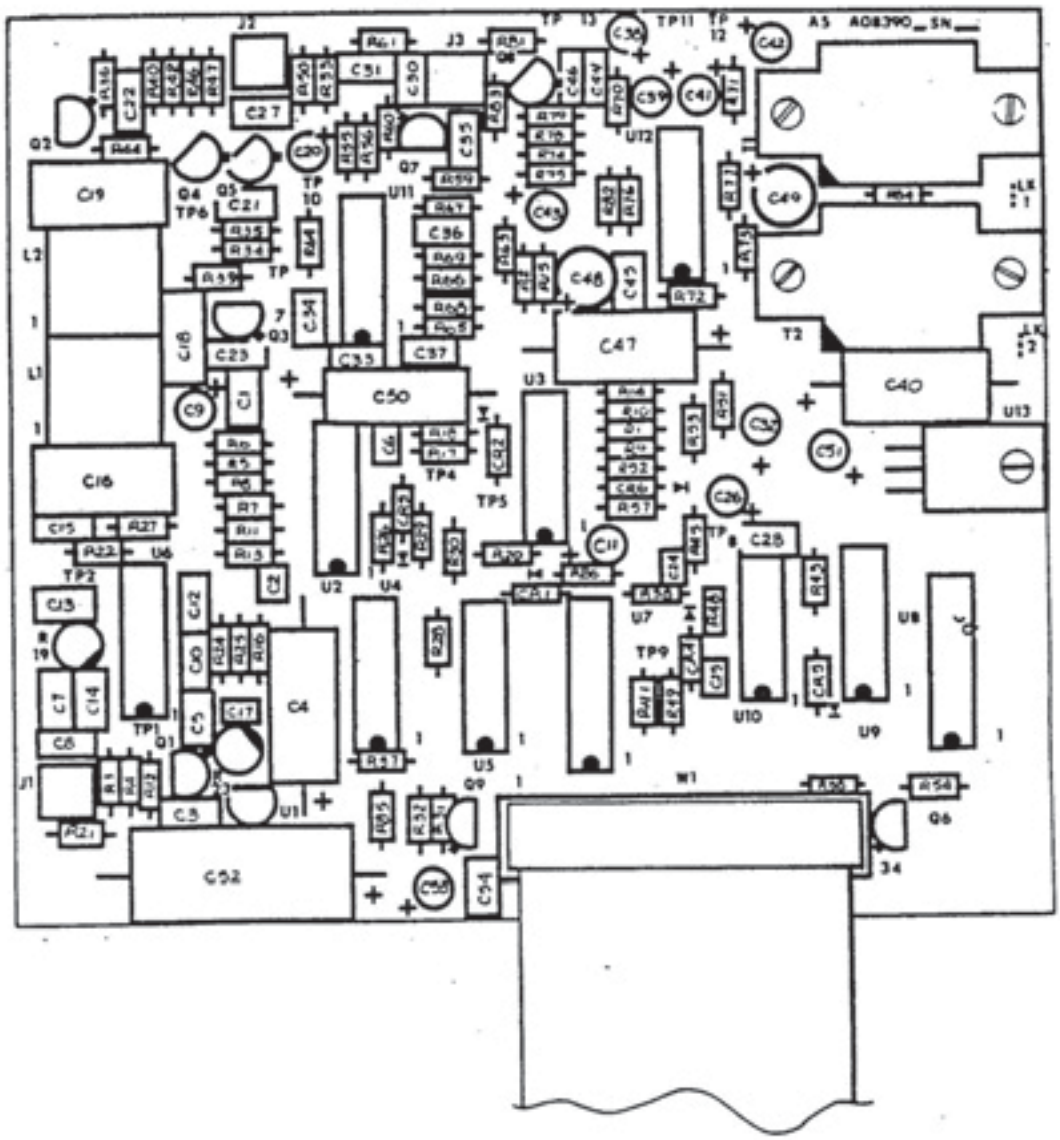

Figure 6-14. Component Location Diagram, A5

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TABLE 6-7. PARTS LIST, ISB CIRCUIT CARD ASSEMBLY, A5

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A5	ISB Circuit Card Assembly	08390	
C1, C3, C5, C7, C8, C10, C12 thru C15, C21, C23, C28, C30, C31, C33 thru C37, C45, C54	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	M39014/01-1593
C2	Capacitor, Ceramic, 1000 pF, 18 WVDC, ±20% (Centralab)	21756	CY15C102M
C4, C50	Capacitor, Electrolytic, 100 uF, 25 WVDC, -10 +50% (Electra)	24066	ET101X025AS
C6	Capacitor, Ceramic, 0.022 uF, 50 WVDC, ±20% (Union Carbide)	21762	C320C223M1U1CA
C9, C26, C53	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20% (Union Carbide)	25062-156	T362B156K020AS
C11, C32, C38, C39, C41, C42, C43, C51	C41 Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C16, C19	Capacitor, Mica, 1500 pF, 500 WVDC, ±2%	22174	CMR06F152GODR
C17, C24, C25	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20% (Union Carbide)	21733	C320C103M1U1C1
C18	Capacitor, Mica, 82 pf, 500 WVDC, ±2%	22108	CMR05E820GODR
C20, C22, C27, C29	Capacitor, not used		
C40, C47	Capacitor, Electrolytic, 220 uF, 16 WVDC, -10 +50% (Electra)	24067	3071FE221T016SF
C44	Capacitor, Ceramic, 4700 pF, 50 WVDC, ±5%	21778	CCR06CG472GR
C46	Capacitor, Ceramic, 2200 pF, 50 WVDC, ±5%	21779	CCR06CG222GR
C48, C49	Capacitor, Tantalum, 68 uF, 15 WVDC, ±20% (Union Carbide)	25063-686	T362C686M015AS
C52	Capacitor, Electrolytic, 470 uF, 25 WVDC, -10 +100% (Electra)	24058	ET471X025A01

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TABLE 6-7. PARTS LIST, ISB CIRCUIT CARD ASSEMBLY, A5 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
CR1 thru CR6	Diode, Silicon	35514	1N916B
J1, J3	Connector, RF (Sealectro)	60044	051-351-0000-220
J2	Connector, not used		
L1, L2	Coil, RF, Variable	08485	
Q1, Q3, Q6, Q7, Q8	Transistor, NPN, High Power	32021	2N5089
Q2, Q4, Q5, Q9	Transistor, not used		
R1, R5, R26, R32, R37, R41, R54, R58	Resistor, Film, 22K, ±2%, 1/4W	12161-223	RLR07C223GR
R2, R18, R38	Resistor, Film, 1.5K, ±2%, 1/4W	12161-152	RLR07C152GR
R3	Resistor, Film, 56K, ±2%, 1/4W	12161-563	RLR07C563GR
R4, R52	Resistor, Film, 12K, ±2%, 1/4W	12161-123	RLR07C123GR
R6, R65, R66, R67, R69	Resistor, Film, 3.3K, ±2%, 1/4W	12161-332	RLR07C332GR
R7, R25, R81	Resistor, Film, 2.2K, ±2%, 1/4W	12161-222	RLR07C222GR
R8, R64	Resistor, Film, 470 ohms, 2%, 1/4W	12161-471	RLR07C471GR
R9, R13, R15, R28	Resistor, Film, 47K, ±2%, 1/4W	12161-473	RLR07C473GR
R10, R11, R14, R29, R34, R35, R43, R56, R63	Resistor, Film, 10K, ±2%, 1/4W	12161-103	RLR07C103GR
R12, R30, R39, R48, R51, R53, R59	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R16, R22	Resistor, Film, 47 ohms, ±2%, 1/4W	12161-470	RLR07C470GR

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TABLE 6-7. PARTS LIST, ISB CIRCUIT CARD ASSEMBLY, A5 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R17, R24	Resistor, Film, 680 ohms, ±2%, 1/4W	12161-681	RLR07C681GR
R19	Resistor, Trimmer, 2K	16090-202	RJ50FP202
R20	Resistor, Film, 330K, ±2%, 1/4W	12161-334	RLR07C334GR
R21	Resistor, Film, 100 ohms, ±2%, 1/4W	12161-101	RLR07C101GR
R23	Resistor, Trimmer, 50K	16090-503	RJ50FP503
R27, R72, R73, R78	Resistor, Film, 4.7K, ±2%, 1/4W	12161-472	RLR07C472GR
R31, R33, R36, R40, R42, R44, R46, R47, R50, R62, R80	Resistor, not used		
R45, R70, R71	Resistor, Film, 15K, ±2%, 1/4W	12161-153	RLR07C153GR
R49	Resistor, Film, 18K, ±2%, 1/4W	12161-183	RLR07C183GR
R55	Resistor, Film, 33K, ±2%, 1/4W	12161-333	RLR07C333GR
R57	Resistor, Film, 6.8K, ±2%, 1/4W	12161-682	RLR07C682GR
R60	Resistor, Film, 33 ohms, ±2%, 1/4W	12161-330	RLR07C330GR
R61	Resistor, Film, 390 ohms, ±2%, 1/4W	12161-391	RLR07C391GR
R68	Resistor, Film, 1.2K, ±2%, 1/4W	12161-122	RLR07C122GR
R74	Resistor, Film, 39K, ±2%, 1/4W	12161-393	RLR07C393GR
R75	Resistor, Film, 68K, ±2%, 1/4W	12161-683	RLR07C683GR
R76, R77	Resistor, Film, 100K, ±2%, 1/4W	12161-104	RLR07C104GR
R79	Resistor, Film, 8.2K, ±2%, 1/4W	12161-822	RLR07C822GR
R82, R84	Resistor, Film, 140 ohms, ±2%, 1/4W	12138	RN55D1400F
R83	Resistor, Film, 22 ohms, ±2%, 1/4W	12161-220	RLR07C220GR
R85	Resistor, Film, 10 ohms, ±2%, 1/4W	12161-100	RLR07C100GR
R86	Resistor, Film, 1 Meg., ±2%, 1/4W	12161-105	RLR07C105GR

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TABLE 6-7. PARTS LIST, ISB CIRCUIT CARD ASSEMBLY, A5 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
T1, T2	Transformer Assembly, Audio	08535	
U1	IC, +12 Volt Regulator (National)	36760	LM78L12AWC
U2	IC, Transistor Array (RCA)	36785	CA3046F
U3, U10	IC, Quad Operational Amplifier (RCA)	36784	CA324E
U4	IC, Dual D Flip-flop	36588	CD4013BE
U5, U9	IC, Quad Bilateral Switch (RCA)	36792	CD4066BE
U6	IC, Operational Amplifier	36541	UA757DMGB
U7, U8	IC, Quad Latch (RCA)	36613	4042B
U11	IC, Product Detector (Motorola)	36748	MC1496L
U12	IC, Dual Audio Amplifier, 2 Watt (National)	36777	LM377N
U13	IC, +15 Volt Regulator (Fairchild)	36708	7815UC
W1	Cable, Ribbon	08486	
W10	Cable Assembly	08555-6	
W11	Cable Assembly, Coaxial	08555-7	

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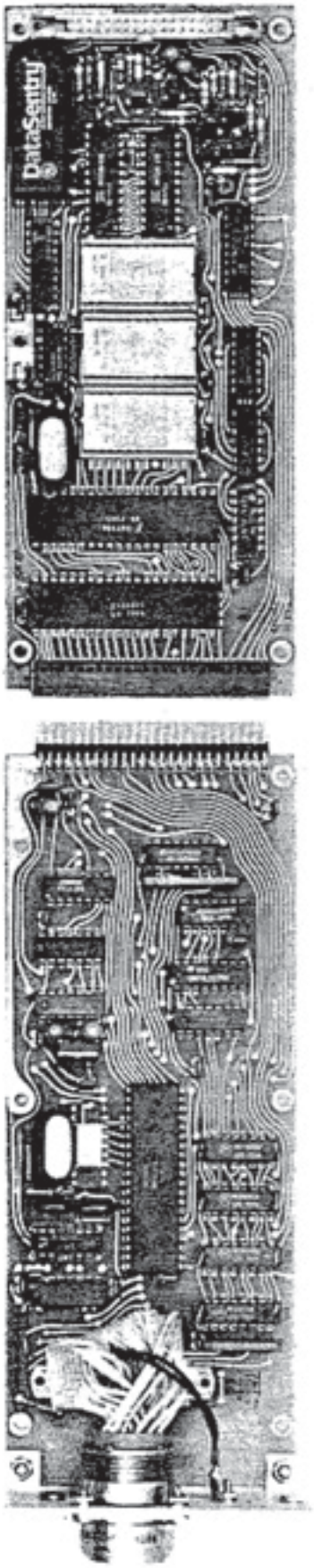

Figure 6-15. Microcomputer Assembly, A6

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TABLE 6-8. PARTS LIST, MICROCOMPUTER ASSEMBLY, A6

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A6	Microcomputer Assembly	08397	
A6A1	Serial Asynchronous Interface Assembly (see Table 6-9 for further breakdown)	08391	
A6A2	Microprocessor Assembly (see Table 6-10 for further breakdown)	08392	
-	ROM Set, R79NRM	08449	

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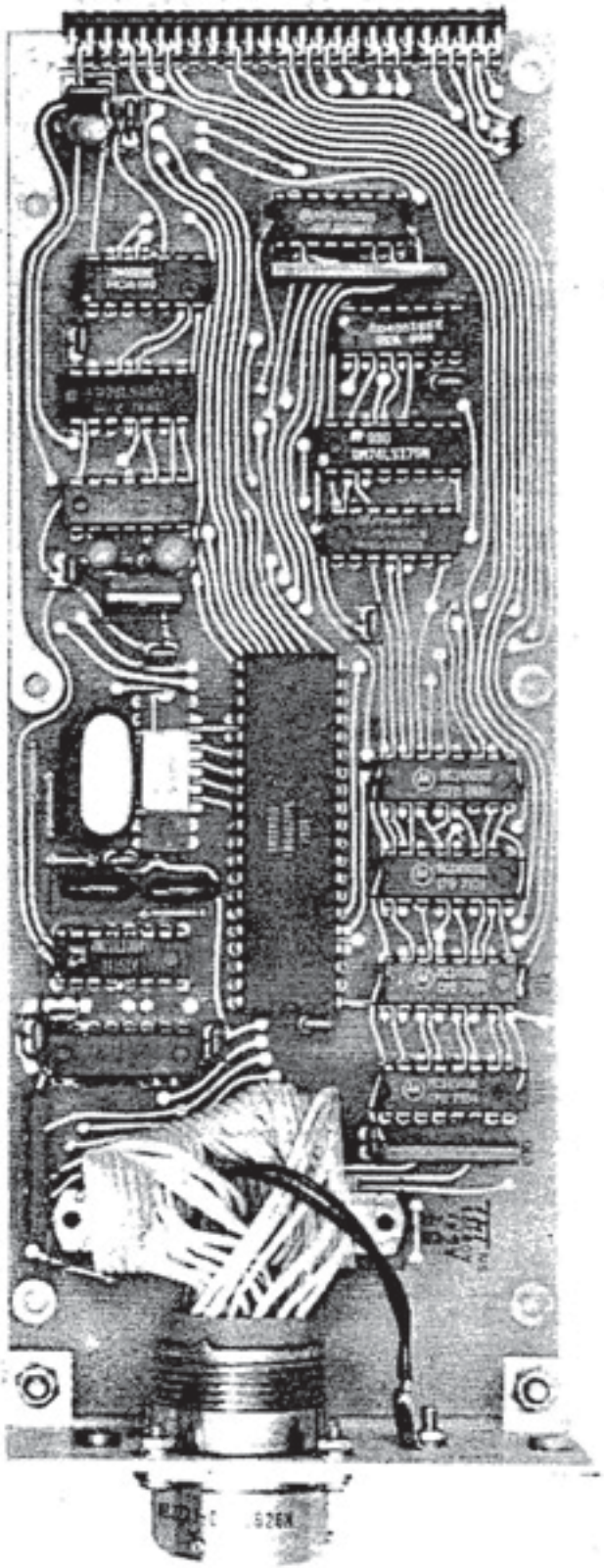

Figure 6-16. Asynchronous Interface Assembly, A6A1

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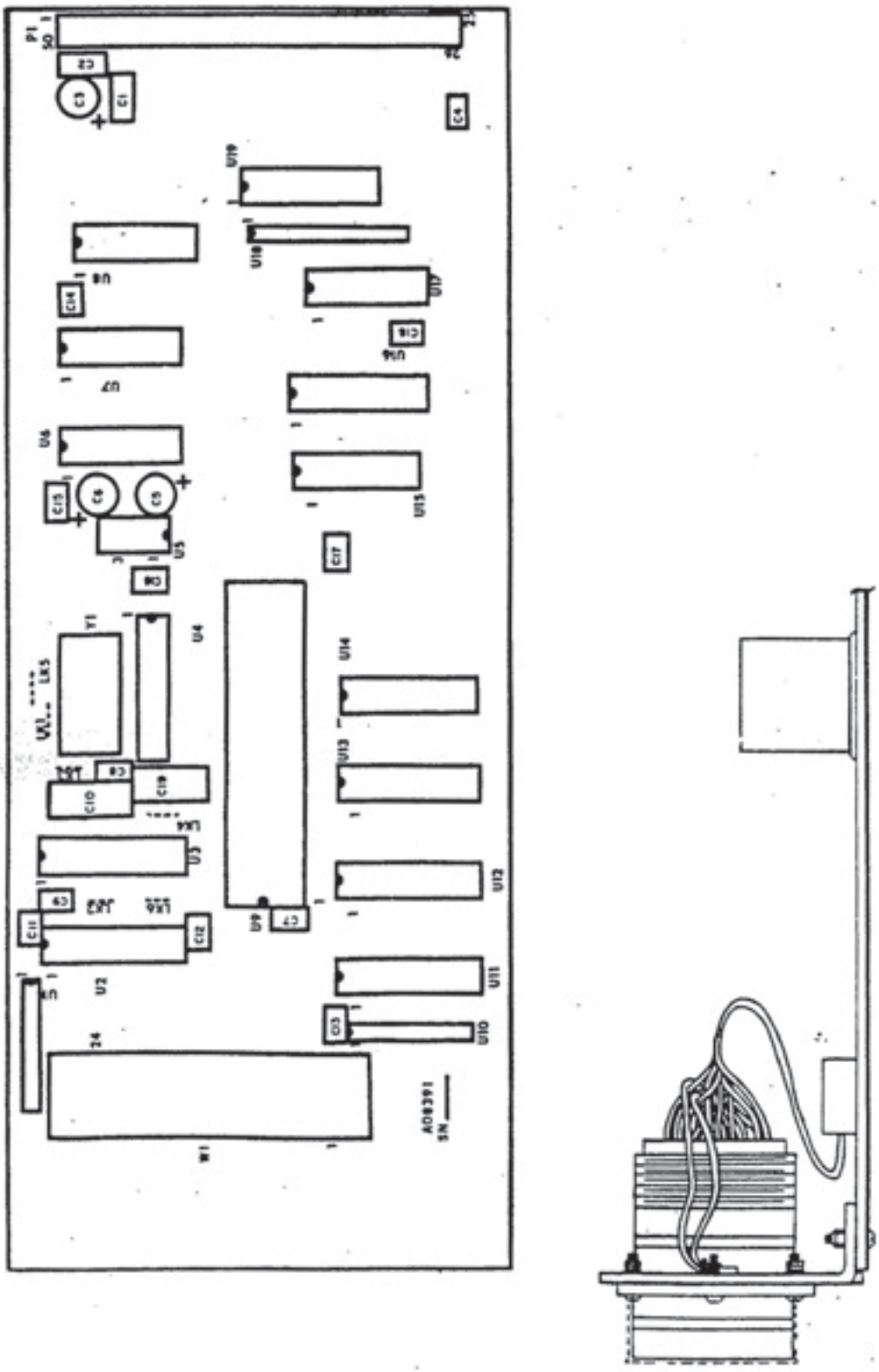

Figure 6-17. Component Location Diagram, A6A1

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TABLE 6-9. PARTS LIST, SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY, A6A1

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A6A1	Serial Asynchronous Interface Assembly	08391	
C1	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	M39014/01-1593
C2	Capacitor, Ceramic, 0.22 uF, 50 WVDC, ±20%	21742	M39014/02-1356
C3	Capacitor, Tantalum, 22 uF, 15 WVDC, ±10% (Union Carbide)	25063-226	T362B226K015AS
C4, C7, C8, C9, C11 thru C18	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20% (Union Carbide)	21733	C320C103M1U1C1
C5, C6	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C10, C19	Capacitor, Mica, 300 pf, 500 WVDC, ±5%	22035	CMR05F301G0DR
P1	Connector, 50-Pin, 2 Section	08491	
U1, U10	Resistor, Network, 22K, 8-Pin, SIP (Dale)	19321-223	SIP-8-223
U2	IC, Quad Differential Line Receiver (Texas Instrument)	36798	AM26LS32CN
U3	IC, Quad RS-423 Line Driver (Advanced Micro)	36797	AM26LS30PC
U4	IC, Baud-Rate Generator (National)	36719	AH5016C-5
U5	IC, -5 Volt Regulator (National)	36704	LM7905CN
U6, U15	IC, Quad 2-Input NAND Gate (Motorola)	36571	MC14011
U7	IC, Hex Inverter	36676	74LS04J
U8	IC, Dual AOI Gates (RCA)	36781	CD4085BF
U9	IC, UART (Siliconix)	36667	JM6402
U11 thru U14	IC, Hex Tri-state Buffer (National)	36694	MC14503BCL
U16	IC, Quad D F/F	36675	74LS175J
U17	IC, Dual 4-Input NOR Gate	36587	MC14002BCL
J18	Resistor Network, 22K, 10-Pin SIP (Bovins)	19323-223	4310R-101-223
U19	IC, Dual 4-Channel Data Select (National)	36650	CD4529BCN

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TABLE 6-9. PARTS LIST, SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY, A6A1 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
W1	Cable Assembly	08493	
W1J1	Connector, 26-Pin, Male, Part of W1	61091	M83723-02R-1626M
-	Connector, 26-Pin, Female, Mates with J1	61092	M83723-13R-1626M
Y1	Crystal, 4.9152 MHz	08490	
-	Plate, Connector Mounting	08471	
-	Dust Cover	64012	MS90376-16Y

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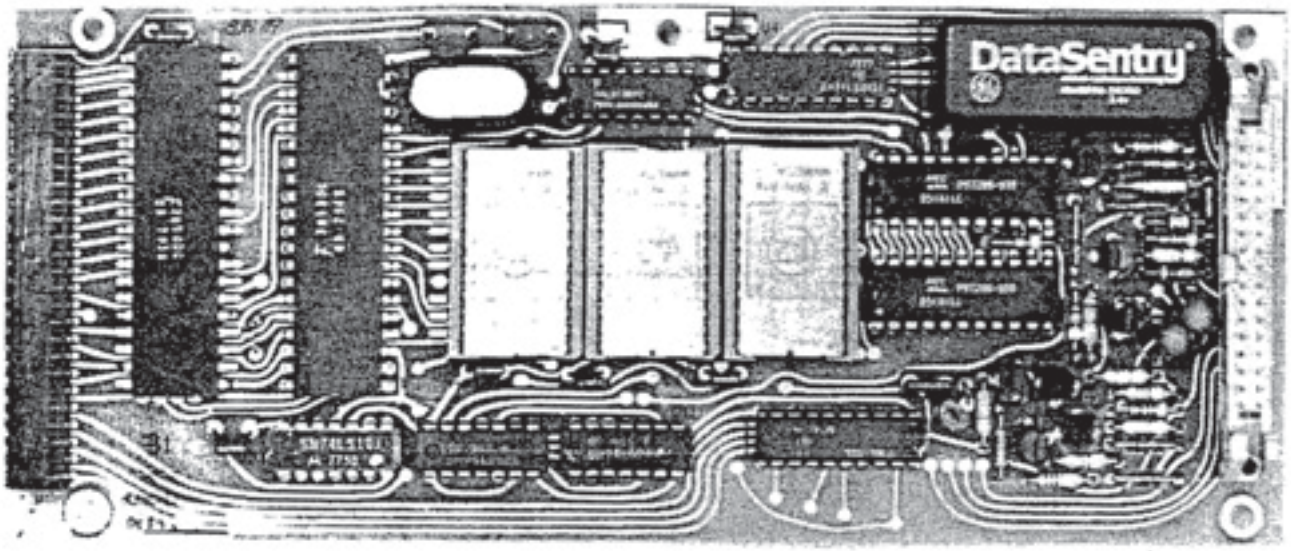

Figure 6-18. Microprocessor Assembly, A6A2

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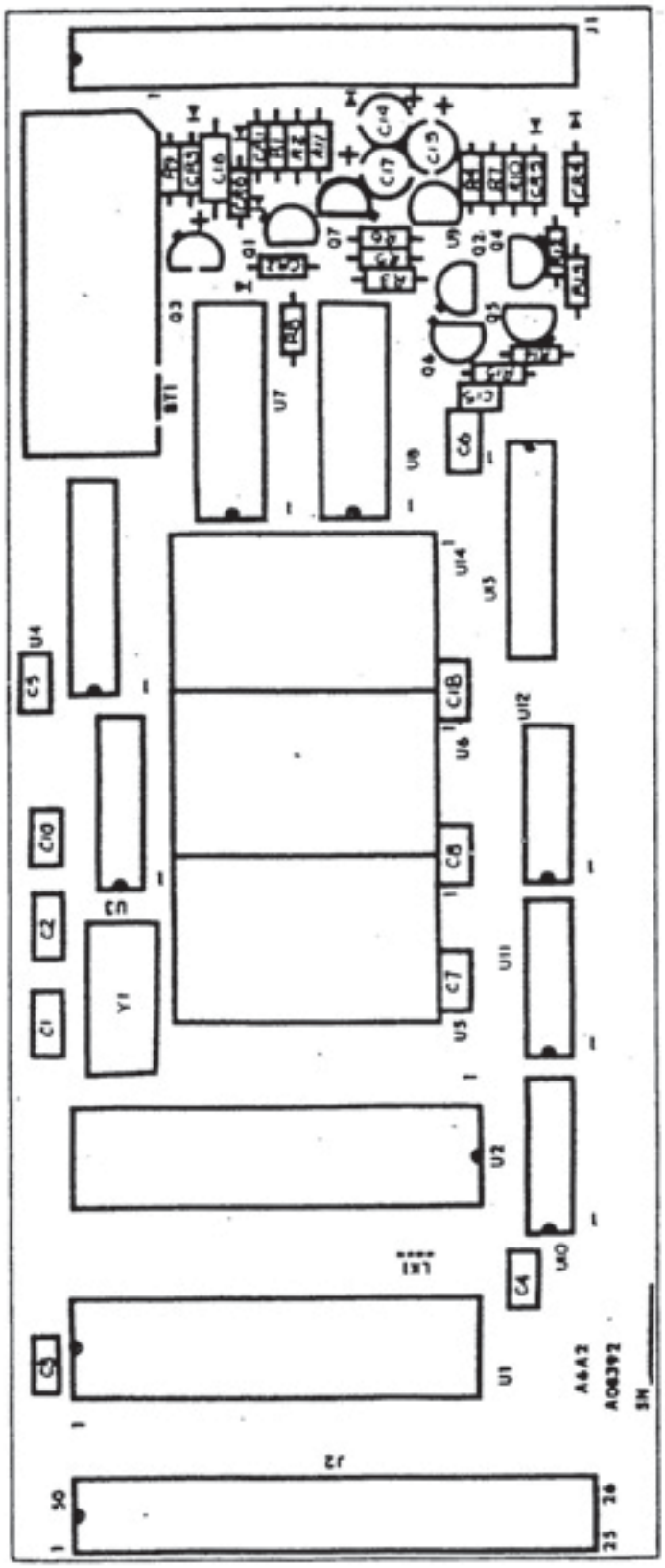

Figure 6-19. Component Location Diagram, A6A2

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TABLE 6-10. PARTS LIST, MICROPROCESSOR ASSEMBLY, A6A2

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A6A2	Microprocessor Assembly	08392	
BT1	Battery, Ni-Cad, 2.4V dc (GE)	42517	DS2SD
C1, C2	Capacitor, Ceramic, 15 pF, Nonpolarized, ±5% (Centralab)	21351	DTZ-15
C3 thru C8, C10, C18	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	M39014/01-1593
C9	Not used		
C13, C14	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C15	Capacitor, Ceramic, 0.001 uF, 50 WVDC, ±20% (Centralab)	21756	CY15C102M
C16	Capacitor, Tantalum, 4.7 uF, 10 WVDC, ±2% (Union Carbide)	25059	T210A475M0L0MS
C17	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20% (Union Carbide)	25062-156	T362B156K020AS
CR1	Diode, Zener, 5.6V dc	33543	1N752A
CR2, CR4, CR5, CR6	Diode, Silicon	35514	1N916B
CR3	Diode, Germanium	35538	1N270
J1	Connector, 34-Pin (3M)	61200	3431-2002
J2	Connector, 50-Pin (Berg)	61225	65000-036
Q1, Q4	Transistor, PNP, Low Power (Motorola)	32037	2N3906
Q2, Q3, Q5	Transistor, NPN, Low Power (Motorola)	32036	2N3904
Q6, Q7	Transistor, Field Effect (Texas Instrument)	32518	TIS74
R1, R7	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R2	Resistor, Film, 39K, ±2%, 1/4W	12161-393	RLR07C393GR
R3, R8	Resistor, Film, 10K, ±2%, 1/4W	12161-103	RLR07C103GR
R4, R12	Resistor, Film, 47K, ±2%, 1/4W	12161-473	RLR07C473GR
R5	Resistor, 120K, ±2%, 1/4W	12161-124	RLR07C124GR

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TABLE 6-10. PARTS LIST, MICROPROCESSOR ASSEMBLY, A6A2 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R6	Resistor, Film, 82K, ±2%, 1/4W	12161-823	RLR07C823GR
R9	Resistor, 270 ohms, ±2%, 1/4W	12161-271	RLR07C271GR
R10, R15	Resistor, Film, 33K, ±2%, 1/4W	12161-333	RLR07C333GR
R11	Resistor, Film, 47 ohms, ±2%, 1/4W	12161-470	RLR07C470GR
R13	Resistor, Film, 10 ohms, ±2%, 1/4W	12161-100	RLR07C100GR
R14	Resistor, Film, 100K, ±2%, 1/4W	12161-104	RLR07C104GR
U1	IC, Central Processor Unit (Mostek)	36710	MK3850
U2	IC, System Memory Interface (Mostek)	36712	MK3853
U3	IC, Dual 1-of-4 Decoder	36671	74LS139
U4	IC, Octal 3-State Transceiver	36741	74LS245
U5, U6, U14	ROM Set, Firmware	08449	2716-2KX8
U7, U8	IC, Random Access Memory (Intel)	36713	P5101L
U9	IC, +12V Regulator, TO-92 (National)	36760	LM78L12AWC
U10	IC, Triple 3-Input NAND Gate	36633	74LS10J
U11	IC, Quad 2-Input NOR Gate	36660	74LS02J
U12	IC, Hex Inverter	36676	74LS04J
U13	IC, Octal D Tri-State F/F	36703	SN74LS374N
XU5, XU6, XU14	IC, Socket, 24-Pin, DIP (Jermyn)	70620	A23-2023Z
Y1	Crystal, 2 MHz	08487	

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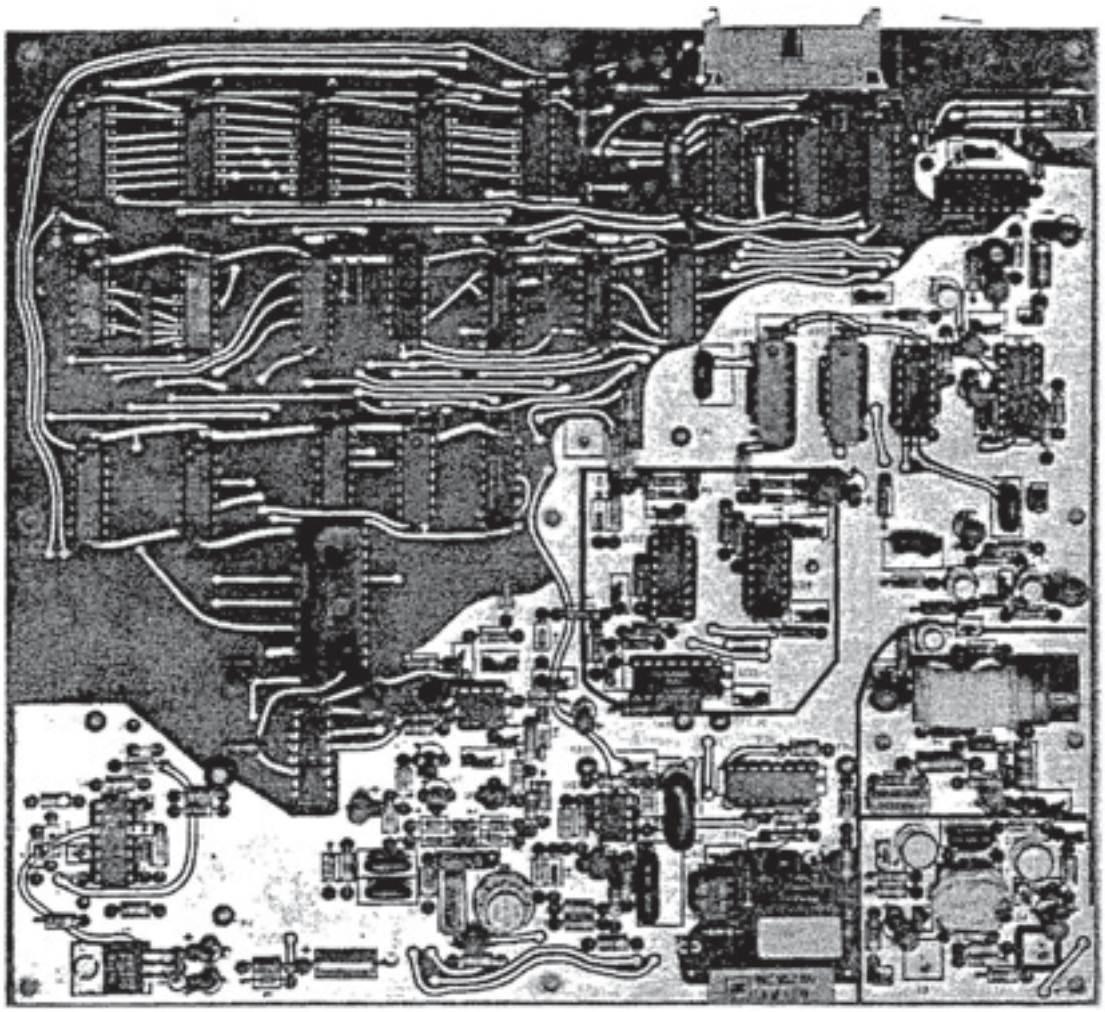

Figure 6-20. First LO Synthesizer Assembly, A7

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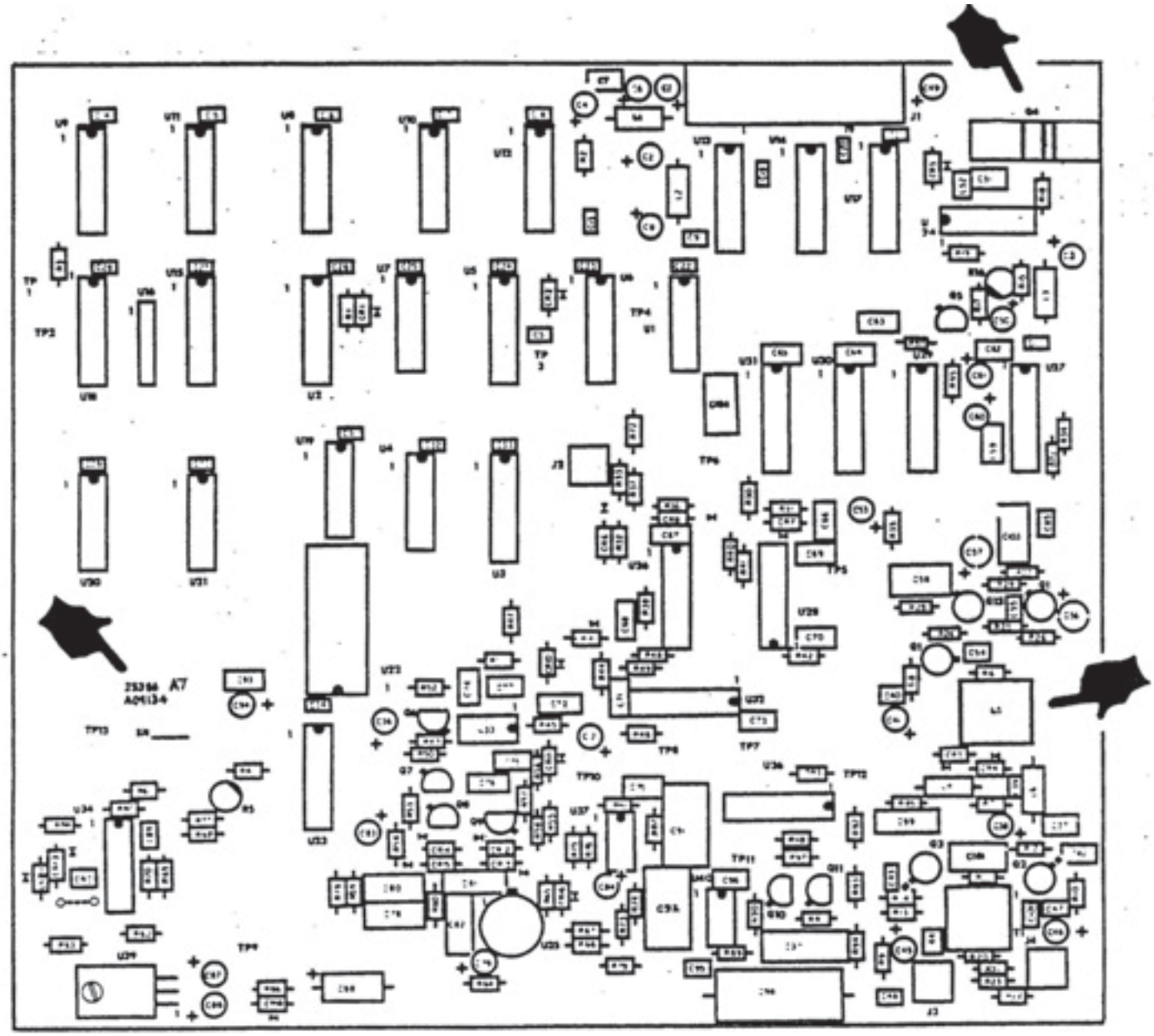

Figure 6-21. Component Location, A7

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TABLE 6-11. PARTS LIST, FIRST LO SYNTHESIZER CIRCUIT CARD ASSEMBLY A7

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A7	First LO Synthesizer Circuit Card Assembly	09134	
C1-C4, C6 C8, C12, C36, C38, C45, C46, C49, C50, C57, C60, C61, C79, C83, C84, C94	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C5, C7, C9, C11, C13-C34, C39, C44, C47, C48, C55, C85	Capacitor, Ceramic, 0.01 uF, 100 WVDC, ±20% (Union Carbide)	21733	8121-050-651-103M
C10, C102	Not Used		
C35, C37, C42, C51, C49, C62 C63-C77, C93, C96	Capacitor, Ceramic, 0.1 uF, 100 WVDC, ±20%	21732	8121-050-651-104M
C40, C43, :52, C54, C95	Capacitor, Ceramic, 0.001 uF, 100 WVDC, ±20% (Centralab)	21756	8101-050-651-102M
C41, C56	Capacitor, Tantalum, 33 uF, 25 WVDC, ±10% (Union Carbide)	25061-336	T362C336M025AS
C53	Capacitor, Tantalum, 150 uF, 6 WVDC, ±20% (Union Carbide)	25065-157	T362C157K006AS
C58	Capacitor, Mica, 10 pF, 500 WVDC, ±5%	22001	CMR05D100G0DR
C78	Capacitor, Mica, 100 pF, 100 WVDC, ±5%	22023	CMR05F101G0DR
C80	Capacitor, Mica, 27 pF, 100 WVDC, ±5%	22119	CMR05E270G0DR
C81	Capacitor, Polyester, 0.001 uF, 400 WVDC, ±10% (Stettner Trush)	26899	KT1806-210/01
C82	Capacitor, Polycarbonate, 0.047 uF, 100 WVDC, ±10% (Electra)	26896	MKC-1862-347/01
C86, C87	Capacitor, Tantalum, 1 uF, 35 WVDC, ±20%	25060-105	T362A105M035AS
C88	Capacitor, Tantalum, 15 uF, 20 WVDC, ±20%	25035	CS13BE156M
C89	Capacitor, Ceramic, 0.047 uF, 100 WVDC, ±20%	27159	8121-050-651-473M
C90	Capacitor, Ceramic, 2200 pF, 100 WVDC, ±20%	21780	8111-100-651-22M
C91	Capacitor, Mica, 4700 pF, 100 WVDC, ±5%	22066	CMR06F472G0DR
C92	Capacitor, Mica, 2200 pF, 100 WVDC, ±%5	22057	CMR06F222G0DR
C97	Capacitor, Polycarbonate, 1.0 uF, 100 WVDC, ±10% (Electra)	26875	C280MCH/A1M
C98	Capacitor, Polycarbonate, 3.3 uF, 63 WVDC, ±10% (Stettner Trush)	26897	MKC-1862-533/06
C99	Capacitor, Polycarbonate, 0.068 uF, 100 WVDC, ±10% (Electra)	26898	MKC-1862-368/01
`100	Capacitor, Ceramic, 4.7 pF (Union Carbide)	21783	8101-100-C0H0479D

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TABLE 6-11. PARTS LIST, FIRST LO SYNTHESIZER CIRCUIT CARD ASSEMBLY A7 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
C101	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	
C103, C104	Capacitor, Mica, 47 pF, 500 WVDC, ±5%	22014	CMR05E470G0DR
CR1, CR2	Diode, Silicon	35514	1N916
CR5-CR16, C19, C20			
CR3, CR4	Diode, Varactor (KSW)	29016	KV2201
CR17, CR21	Diode, Not Used		
CR18	Diode, Zener, 9.1 V	33544	1N757A
J1	Connector, PCB, Right Angle, 20-Way (3M)	61276	3492-1002
J2, J3, J4	Connector, PCB, Coaxial, SMB, Male (Sealectro)	60044	051-851-0000-91
L1-L4	Choke, Fixed, RF, 6.8 uH, ±10%	43028	LT10K129
L5	Coil Assembly, Air-Wound LO Coil, Variable	D09255	
L6	Choke, Fixed, RF, 15 uH, ±10%	43040	LT10K133
Q1	Transistor, Field Effect	32508	2N4416
-	Pad, Transistor, Q1, Q5, Q12, Q13	70752	7717-7NWHT
Q2, Q3	Transistor, NPN, RF High Power	32044	MRF517
-	Pad, Transistor, Q2, Q3	70764	N88226
Q4	Transistor, NPN, High Power (Motorola)	30239	2N4921
-	Pad, Transistor, Q4	70770	RC-T05140-8A
Q5, Q13	Transistor, NPN, Silicon	32255	2N2369
Q6, Q7, Q8, Q11	Transistor, PNP, Silicon (Motorola)	31508	2N4126
Q9, Q10	Transistor, NPN, Low Power (Motorola)	32035	2N4124
Q12	Transistor, NPN, Low Power, Silicon	31500	2N918
R1, R87, R89	Resistor, Film, 47K, ±2%, ¼W	12161-471	RL407C473GR
R2, R12, R28, R72, R92, R94	Resistor, Film, 10 ohms, ±2%, ¼W	12161-100	RLR07C100GR
R3, R50, R62, R73, R81, R82, R83	Resistor, Film, 10K, ±2%, ¼W	12161-103	RLR07C103GR
R4, R91	Resistor, Film, 150 ohms, ±2%, ¼W	12161-151	RLR07C151GR
R5	Resistor, Variable, 200 ohms	16090-201	RJR50FP201
R6, R29, R85	Resistor, Film, 100 ohms, ±2%, ¼W	12161-101	RLR07C101GR
R7, R8, R14, R23	Resistor, Film, 68 ohms, ±2%, ¼W	12161-680	RLR07C680GR
R9, R22, R60	Resistor, Film, 22 ohms, ±2%, ¼W	12161-220	RLR07C220GR
R10, R26	Resistor, Film, 1.5K, ±2%, ¼W	12161-152	RLR07C152GR
R11, R93	Resistor, Film, 680 ohms, ±2%, ¼W	12161-681	RLR07C681GR
R13	Resistor, Film, 390 ohms, ±2%, ¼W	12161-391	RLR07C391GR
R15, R30, R33, R37, R47	Resistor, Film, 820 ohms, ±2%, ¼W	12161-821	RLR07S821GR
R16	Resistor, Variable, 500 ohms	16090-501	RJR50FP501

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TABLE 6-11. PARTS LIST, FIRST LO SYNTHESIZER CIRCUIT CARD ASSEMBLY A7 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R17, R52, R56	Resistor, Film, 2.2K, ±2%, ¼W	12161-222	RLR07C222GR
R18	Resistor, Film, 47 ohms, ±2%, ¼W	12161-470	RLR07C470GR
R19	Resistor, Composition, 1 ohm, ±5% (Stettner Trush)	12153	SK2-2/4-1R0J
R20	Resistor, Film, 39 ohms, ±2%, ¼W	12161-390	RLR07C390GR
R21, R27	Resistor, Film, 330 ohms, ±2%, ¼W	12161-331	RLR07C331GR
R24, R34, R35, R38, R40-R44, R46, R48, R49, R55, R58, R86	Resistor, Film, 470 ohms, ±2%, ¼W	12161-471	RLR07C471GR
R25, R61, R63, R68, R70, R90, R95, R97	Resistor, Film, 1K, ±2%, ¼W	1216-102	RLR07C102GR
R31, R32, R36	Resistor, Film, 220 ohms, ±2%, ¼W	12161-221	RLR07C221GR
R39	Resistor, not used		
R45	Resistor, Film, 56K, ±2%, ¼W	12161-563	RLR07C563GR
R51	Resistor, Film, 4.7K, ±2%, ¼W	12161-472	RLR07C472GR
R53, R54, R59, R69, R84	Resistor, Film, 3.3K, ±25, ¼W	12161-332	RLR07C332GR
R57	Resistor, Film, 3.9K, ±2%, ¼W	12161-392	RLR07C392GR
R64	Resistor, Film, 39K, ±2%, ¼W	12161-393	RLR07C393GR
R65, R74, R75, R76	Resistor, Film, 15K, ±2%, ¼W	12161-153	RLR07C153GR
R66	Resistor, Film, 8.2K, ±2%, ¼W	12161-822	RLR07C822GR
R67, R79	Resistor, Film, 12K, ±2%, ¼W	12161-123	RLR07C123GR
R71	Resistor, Film, 82 ohms, ±2%, ¼W	12161-820	RLR07C820GR
R77	Resistor, Film, 100K, ±2%, ¼W	12161-104	RLR07C104GR
R78	Resistor, Film, 2.7K, ±2%, ¼W	12161-272	RLR07C272GR
R80	Resistor, Film, 150K, ±2%, ¼W	12161-154	RLR07C154GR
R88	Resistor, Film, 120K, ±2%, ¼W	12161-124	RLR07C124GR
T1	Transformer, Wideband	08502-1	
U1	IC, Quad 2-Input NOR Gate (Motorola)	36569	M38510/0520BCB
U2	IC, Hex 3-State Buffer (Motorola)	36694	MC14503BCL
U3, U5, U6	IC, 6-Bit D Flip-Flop	36715	M38510/30106BEB
U4	IC, Quad 2-Input NOR Gate	36660	M38510/30301BCB
U7	IC, Quad Exclusive NOR Gate (Motorola)	36653	4070BCL
U8-U14	IC, 8-Bit Register, Shift and Store (RCA)	36767	CD4094BE
U15	IC, 4-Bit BCD Adder (Signetics)	36768	N82S83N
U16	IC, Resistor Array, 6-Pin, 10K (Bovins)	19324-103	4306R-101-103
U17	IC, 4-Bit Full Adder (Motorola)	36570	M38510/05401BCB
U18	IC, Hex D Flip-flop (RCA)	36766	40/74B
U19	IC, Dual D Flip-flop	36636	M38510/30102BCB

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TABLE 6-11. PARTS LIST, FIRST LO SYNTHESIZER CIRCUIT CARD ASSEMBLY A7 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
U20, U21	IC, 18 Bit Static Shift Register (Motorola)	36769	M38510/05710BCB
U22	IC, 4x4 Multiport Register (RCA)	36770	CD40108BE
U23	IC, Digital to Analog Converter (PMI)	36771	DAC20CQ
U24	IC, Voltage Regulator (Fairchild)	36728	M38510/10201BEA
U25, U38	IC, not used		
U26, U28	IC, Dual D Flip-flop (Fairchild)	36774	10231DC
U27	IC, Divide by 10/11 Prescaler (Fairchild)	36745	11C90
U29	IC, Binary Up-Down Counter	36772	M38510/31506BEA
U30, U31	IC, Decode, Up-Down Counter	36773	M38510/31506BEA
U32	IC, Dual 2-Input NOR Gate (Fairchild)	36775	10211DC
U33, U37	IC, Dual Operational Amplifier (National)	36776	LM1458N
U34	IC, Quad Voltage Comparator	36693	M38410/11201BCB
U35	IC, Operation Amplifier (Analog Device)	36765	AD518JH
U36	IC, Analog Switch (Analog Device)	36815	DG201
U39	IC, +12 Volt Regulator (Fairchild)	36707	M38510/1070BYB
U40	IC, Operational Amplifier (Intersil)	36817	CA3140E

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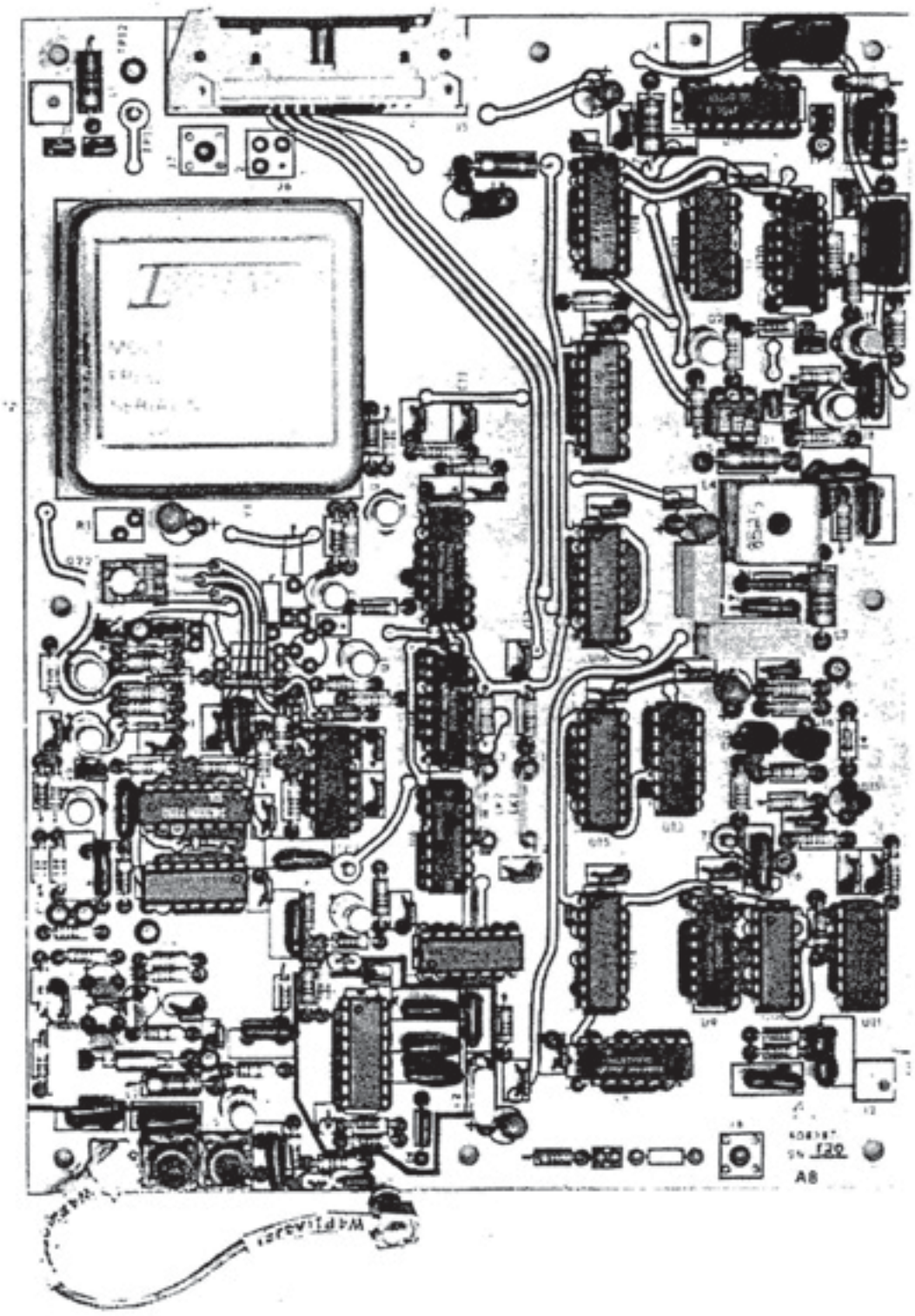

Figure 6-22. Second LO/BFO Synthesizer, A8

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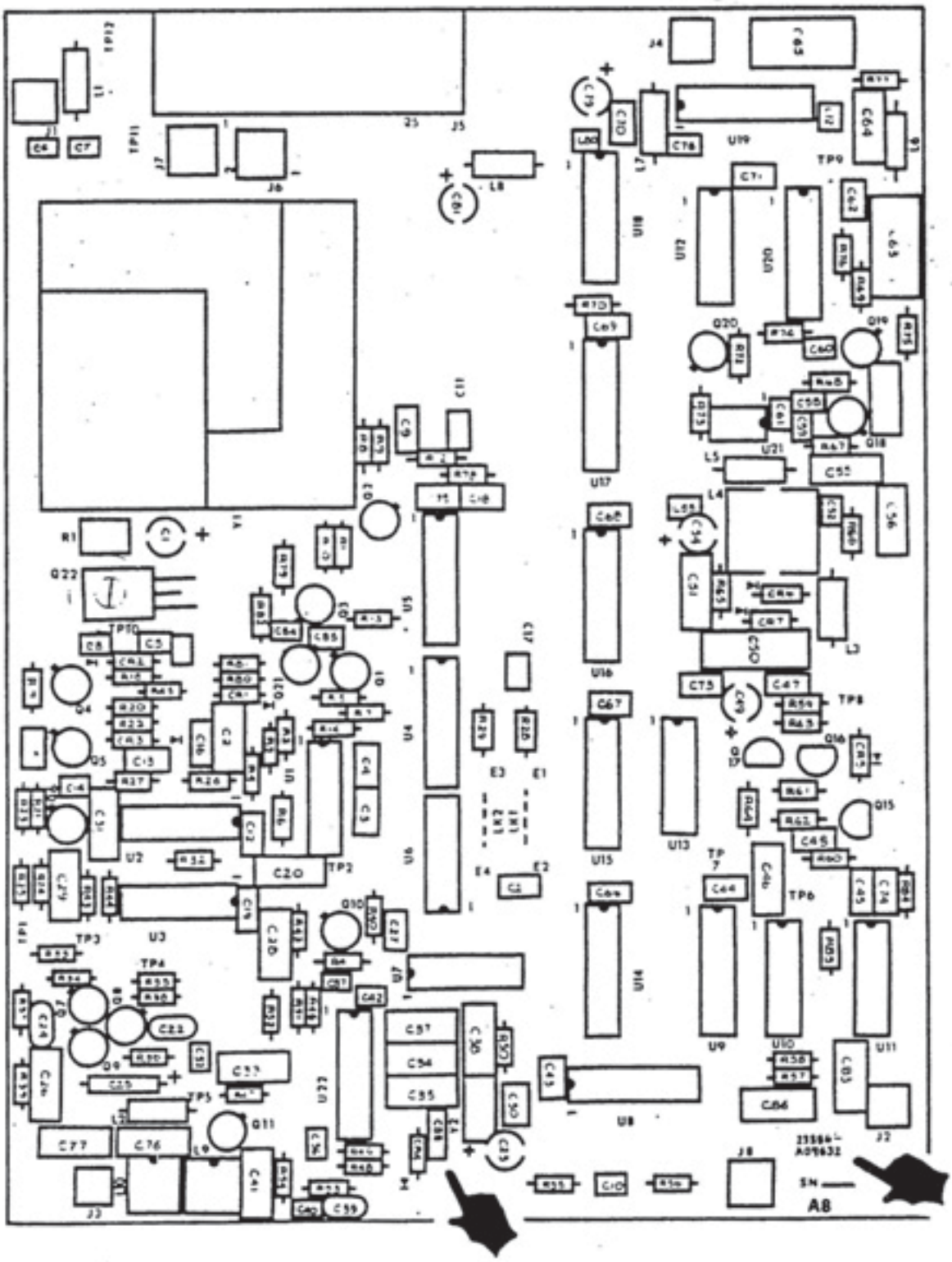

Figure 6-22. Component Location, A8

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TABLE 6-12. PARTS LIST, SECOND LO/BFO SYNTHESIZER CIRCUIT CARD ASSEMBLY, A8

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A8	Second LO/BFO Synthesizer Assembly	09632	
C1, C23 C49, C54, U79, C81	Capacitor, Tantalum, 6.8 uF, 35 WVDC, (Union Carbide)	25060-685	T362A685M035AS
C2, C34, C35, C37, C46, C56, C57	Capacitor, Mica, 100 pF, 500 WVDC, ±5%	22023	CMR05F101G0DR
C3, C4, C9, C11, C12, C13, C15-C19, C21, C22, C24, C27, C30, C39, C43, C44, C45, C47, C48, C62, C66-C71, C73, C74	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	M39014/01-1593
C5, C8, C32, C42, C52, C53, 58-C61, C72, C78, C80, C14	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20% (Union Carbide)	21733	C320C103M1U1C1
C6, C7	Capacitor, Ceramic, 0.047 uF, 50 WVDC, ±20% (Union Carbide)	21759	C320C473M5U1CA
C82, C84, C85	Capacitor, not used		
C20	Capacitor, Mica, 12 pF, 500 WVDC, ±10%	22002	CMR05C120G0DR
C25	Capacitor, Tantalum, 3.3 uF, 15 WVDC, ±20%	25066	CS13BE335M
C26, C51	Capacitor, Polycarbonate, 0.1 uF, 100 WVDC, ±10% (Electra)	26871	C280MCH/A100K
C28, C64	Capacitor, Mica, 150 pF, 500 WVDC, ±2%	22101	CMR05F151G0DR
C29, C31, C83, C86	Capacitor, Mica, 39 pF, 500 WVDC, ±2%	22100	CMR05F301G0DR
C33, C41	Capacitor, Mica, 68 pF, 500 WVDC, ±2%	22107	CMR05E680G0DR
C36, C40, C87, C10	Capacitor, Ceramic, 0.001 uF, 50 WVDC, ±20% (Centralab)	21756	CY15C102M
C38, C88	Capacitor, Mica, 5 pF, 500 WVDC, ±½ pF	22175	CMR05C5R0D0DR
C50	Capacitor, Polycarbonate, 0.47 uF, 100 WVDC, ±20%, (Electra)	26874	C280MCH/A470K
C55	Capacitor, Mica, 56 pF, 500 WVDC, ±5%	22017	CMR05E560J03
C63, C65	Capacitor, Mica, 820 pF, 500 WVDC, ±5%	22047	CMR06F821J0DR
C75	Capacitor, Ceramic, 1.0 uF, 50 WVDC, ±2%	21748	M39014/02-1419
C76	Capacitor, Mica, 82 pF, 500 WVDC, ±2%	22108	CMR05E820G0DR
C77	Capacitor, Mica, 330 pF, 500 WVDC, ±2%	22117	CMR05F331G0DR
CR1	Diode	35525	1N4001

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TABLE 6-12. PARTS LIST, SECOND LO/BPO SYNTHESIZER CIRCUIT CARD ASSEMBLY, A8 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
CR2, CR3, CR5	Diode, Silicon	35514	1N916B
CR4	Diode, Varicap (Motorola)	29013	MV1634
CR6, CR7	Diode, Varicap (Motorola)	29006	MV1650
J1-J4	Connector, SMB, Push-on (Sealectro)	60044	051-851-0000-220
J8, J9			
J5	Connector, 26-Pin, Right-Angle Control/ Power (3M)	61228	3429-1002
J6, J7	Connector, not used		
L1	Inductor, RF, 100 uH, ±10%	43033	LT19K012
L2	Inductor, RF, 1 uH, ±10%	43024	LT4K081
L3, L5	Inductor, RF, 33 uH, ±10%	43031	LT10K138
L4	Inductor, Variable	08525	
L6	Inductor, RF, 220 uH, ±10%	43034	LT10K020
L7, L8	Inductor, RF, 5.6 uH, ±20%	43027	LT10K128
L9, L10	Inductor, Variable	08522	
Q1-Q6	Transistor, NPN	32255	2N2369
Q10, Q11, Q20			
-	Switching Pad, Transistor, Q1-Q6, Q10, Q11, Q18, Q19, Q20	70752	
Q7, Q9, Q15, Q17	Transistor, NPN, Low Power (Motorola)	32036	2N3904
Q8, Q16	Transistor, PNP, Low Power (Motorola)	31508	2N4126
Q18, Q19	Transistor, Field Effect	32524	2N4416A
Q22	Transistor, NPN, High Power (Motorola)	32039	2N4921
-	Pad, Transistor, Q22	70793	
Q12, Q13, Q14, Q21	Transistor, not used		
R1, R15, R16, R17, R30, R31, R71, R79, R80, R81, R82, R70	Resistor, not used		
R2	Resistor, Film, 1 ohm, ±5%, ¼W (Gyrex)	12153	SK2-1/4-1R0J
R3	Resistor, Film, 3.9K, ±2%, ¼W	12161-392	RLR07C392GR
R4	Resistor, Film, 6.8K, ±2%, ¼W	12161-682	RLR07C682GR
R5, R39, R60, R64	Resistor, Film, 2.2K, ±2%, ¼W	12161-222	RLR07C222GR
R6, R33, R34, R38, R59, R63, R67	Resistor, Film, 680 ohms, ±2%, ¼W	12161-681	RLR07C681GR
R7, R24, R25, R72	Resistor, Film, 4.7K, ±2%, ¼W	12161-472	RLR07C472GR
R8, R14, R32, R83, R56	Resistor, Film, 47 ohms, ±2%, ¼W	12161-470	RLR07C470GR

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TABLE 6-12. PARTS LIST, SECOND LO/BFO SYNTHESIZER CIRCUIT CARD ASSEMBLY, A8 (Cont)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R9	Resistor, Film, 33 ohms, ±2%, ¼W	12161-330	RLR07C330GR
R10, R13, R23, R41, R43, R44, R45, R48, R49, R54, R57, R58, R74, R84	Resistor, Film, 1K, ±2%, ¼W	12161-102	RLR07C102GR
R11, R27, R69	Resistor, Film, 330 ohms, ±2%, ¼W	12161-331	RLR07C331GR
R12, R26	Resistor, Film, 10 ohms, ±2%, ¼W	12161-100	RLR07C100GR
R18, R20, R37, R62	Resistor, Film, 3.3 K, ±2%, ¼W	12161-332	RLR07C332GR
R19, R21, R75	Resistor, Film, 1.8K, ±2%, ¼W	12161-182	RLR07C182GR
R22, R35, R76, R77	Resistor, Film, 820 ohms, ±2%, ¼W	12161-821	RLR07C821GR
R28, R29, R36, R47, R61, R73, R78	Resistor, Film, 10K, ±2%, ¼W	12161-103	RLR07C103GR
R40, R42, R50, R51, R55	Resistor, Film, 470 ohms, ±2%, ¼W	12161-471	RLR07C471GR
R46	Resistor, Film, 56 ohms, ±2%, ¼W	12161-560	RLR07C560GR
R52	Resistor, Film, 220 ohms, ±2%, ¼W	12161-221	RLR07C221GR
R53	Resistor, Film, 100 ohms, ±2%, ¼W	12161-101	RLR07C101GR
R65	Resistor, Film, 18K, ±2%, ¼W	12161-183	RLR07C183GR
R66, R68	Resistor, Film, 560K, ±2%, ¼W	12161-564	RLR07C564GR
U1	IC, Voltage Regulator (Fairchild)	36728	UA723
U2	IC, Quad 2-Input NAND Gate	36632	74LS00
U3, U7	IC, Dual D Flip-flop	36636	74LS74
U10	IC	36884	MS38510
U4, U5	IC, Data Selector	36743	74LS151
U6	IC, Decade Counter (Fairchild)	36637	74LS90
U8, U9, U20	IC, Dual Decade Counter (National)	36744	74LS390
U11	IC, Quad 2-Input NAND Gate (National)	36809	DM74LS00NAT
U12	IC, Quad 2-Input NOR Gate	36660	74LS02
U13	ID, Quad 2-Input NAND Gate	36734	74LS08
U14-U18	IC, Synchronous 4-Bit Counter	36702	74LS160
U19	IC, Divide by 10/11 Prescaler (Fairchild)	36745	11C90DCQR
U21	IC, not used		
U22	IC, ECL Line Receiver (National)	36805	DM10115N
Y1	Oscillator, OCXO	08289	
Y2	Crystal, 20 MHz	37039	PEL-18PCR 78/U

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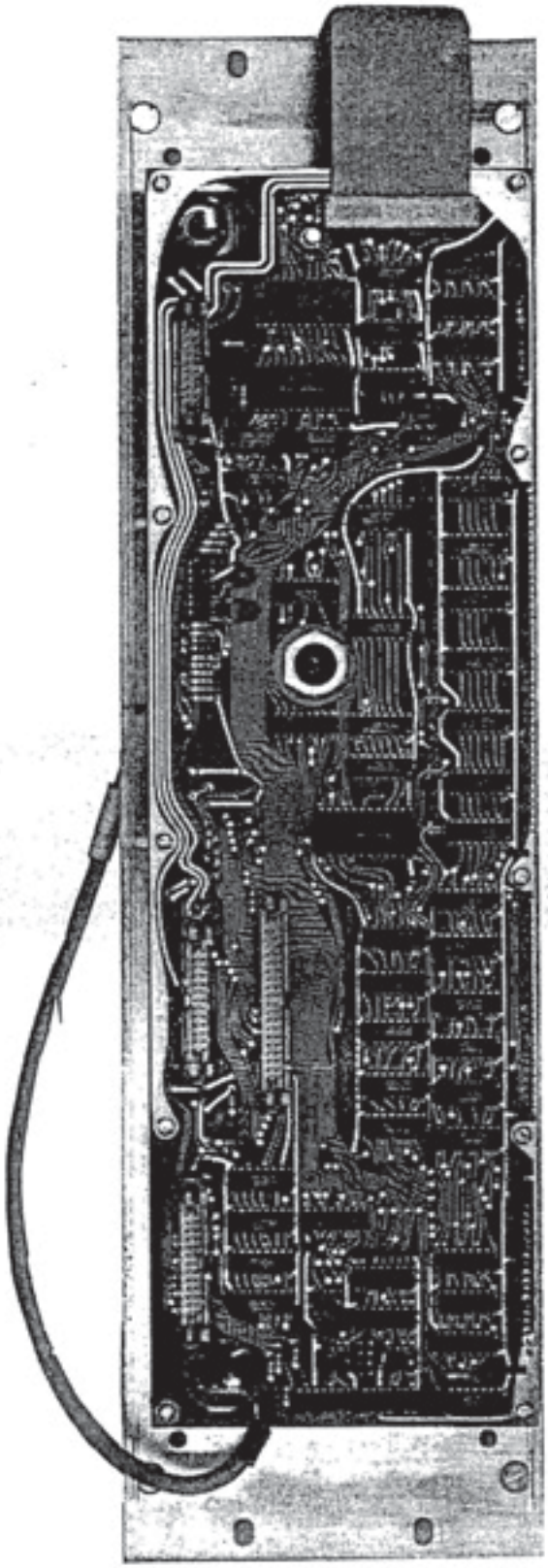

Figure 6-24. Receiver Control Assembly, A9

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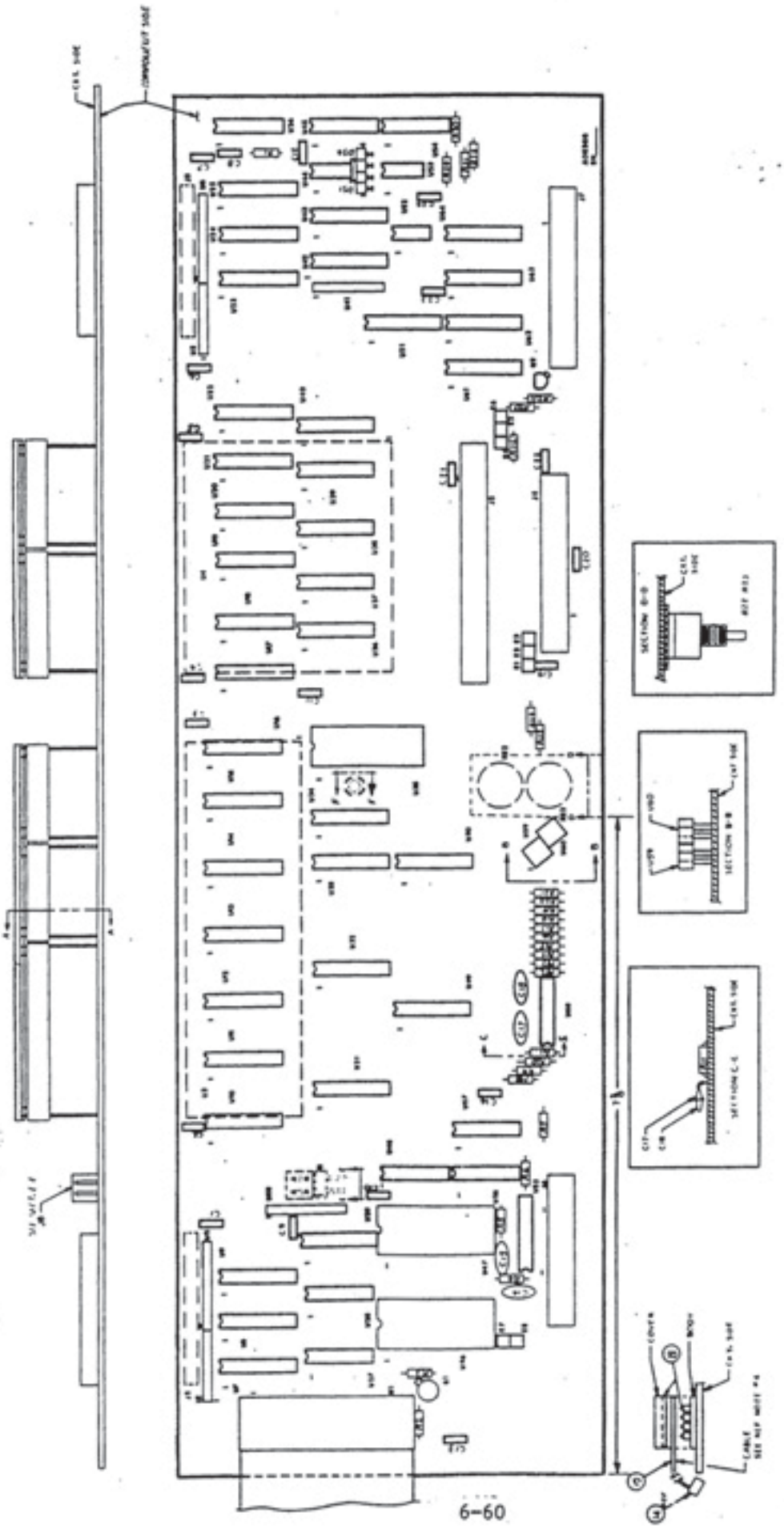

Figure 6-25. Component Location, A9

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TABLE 6-13. PARTS LIST, RECEIVER CONTROL ASSEMBLY, A9

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A9	Receiver Control Assembly	08388	
C1 thru C7, C9 thru C13 C16, C19 thru C24	Capacitor, Ceramic 0.01 uF, 50 WVDC, ±20% (Union Carbide)	21733	8121-050-651-103M
C8	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	8131-050-651-104M
C14, C15	Capacitor, Ceramic, 20 pF, Nonpolarized, ±5% (Centralabl)	21352	DTZ-20
C17, C18	Capacitor, Ceramic, 100 pF, Nonpolarized, ±10%	21763	831-000-X5F0-101K
DS1 thru DS4	LED/Resistor Assembly (HP)	41018	HLMP6620
DS5	LED/Resistor Assembly (HP)	41026	HP5082-4468
J2, J3	Connector, 17 Contact, Switch Panel (Burndy)	61240	HPLB17S-5
J4, J7	Connector, 26 Contact, BFO, Power (3M)	61231	3429-2002
J5	Connector, 40 Contact, IF (3M)	61230	3432-2002
J6	Connector, 20 Contact, Synthesizer (3M)	61213	3428-2002
J8	Connector, 4 Contact	08573	
P1	Connector, 34 Contact, P/O W1 (3M)	61246	3402-000UT
Q1	Transistor, NPN, Switching	32255	2N23b9
-	Pad, Transistor, Q1	70752	7177-7N WHT
Q2	Transistor, PNP, Low Power (Motorola)	32037	2N3906
R1	Resistor, Film, 20K, ±2%, 1/4W	12161-203	RLR07C203GR
R2, R6, R27, R28	Resistor, Film, 10K, ±2%, 1/4W	12161-103	RLR07C103GR
R3, R14, R15	Resistor, Film, 1K, ±2%, 1/4W	12161-102	RLR07C102GR
R4, R5	Resistor, Film, 33K, ±2%, 1/4W	12161-333	RLR07C333GR
R7	Resistor, Film, 100 ohms, ±2%, 1/4W	12161-101	RLR07C101GR

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TABLE 6-13. PARTS LIST, RECEIVER CONTROL ASSEMBLY, A9 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
R8, R9, R24, R25	Resistor, Film, 3.9K, ±2%, 1/4W	12161-392	RLR07C392GR
R10, R11	Resistor, Film, 11K, ±2%, 1/4W	12161-113	RLR07C113GR
R12, R13	Resistor, Film, 1 Meg. ohm, ±2%, 1/4W	12161-105	RLR07C105GR
R16, R17	Resistor, Film, 100K ohm, ±2%, 1/4W	12161-104	RLR07C104GR
R18, R19, R29 thru R32	Resistor, Film, 22K ohm, ±2%, 1/4W	12161-223	RLR07C223GR
R20, R21	Resistor, Film, 180 ohms, ±2%, 1/4W	12161-181	RLR07C181GR
R22, R23	Potentiometer, 25K, audio Line	08473	
R26	Resistor, Film, 15K ohm, ±2%, 1/4W	12161-153	RLR07C153GR
U1, U5	IC, Resistor Array, 10K	19321-103	750-81-R10K
U2, U6, U30	IC, Resistor Array, 10K (Bovins)	19323-103	4310R-101-103
U3	IC, LCD, Frequency	08270	
U4	IC, LCD, Function	08526	
U7, U8, U9, U23, U24, U25, U42, U43	IC, Hex 3-State Buffer (Motorola)	36694	MC14503BCL
U10 thru U18, U31 thru U34	IC, Display Drivers, 7 Segment (RCA)	36752	4056B
U19 thru U22, U36 thru U40, U49	IC, Display Drivers, 4 Line (RCA)	36750	4054B
U26	IC, Monstable/Astable Multivibrator	36786	4047B
U27, U28	IC, Quad Bilateral Switch (RCA)	36792	CD4066BE
U29	IC, 8-Channel Analog Multiplexer (Motorola)	36687	4051B
U35, U47	IC, Address Decoder (RCA)	36751	4514B
U41	IC, Resistor Array, 22K (Dale)	19321-223	SIP-8-223

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TABLE 6-13. PARTS LIST, RECEIVER CONTROL ASSEMBLY, A9 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
U44, U52, U53	IC, Dual 2-Input NAND Buffer/Driver (RCA)	36795	40107B
U45, U54	IC, Dual D Flip-flop (RCA)	36588	M38510/05101BCA
U46	IC, Dual 4-Bit Latch (RCA)	36810	4508B
U48	IC, Triple 3-Input NOR Gate	36649	M38510/05204BCB
U50	IC, Decimal Decoder (Motorola)	36575	MC14028BCL
U51	IC, Up-Down Counter (National)	36583	MC14516BCL
U55	IC, One-Shot Multivibrator (RCA)	36611	4528
U56	IC, Hex Inverter (RCA)	36685	MC14069BCL
U57	IC, Quad 2-Input AND Gate (Motorola)	36677	M38150/17001BCD
U58	IC, Quad Voltage Comparator	36693	M38510/11201BCB
U59, U60	IC, Optical Transducer (Optron)	36754	OPB706A
U61 thru U64	IC, 8-Bit Addressable Latch	36808	4099B
W1	Cable Assembly	08536	
-	Connector, 34 Contact, P/O W1 (3M)	61197	3414-6034
-	Socket, SIP, 11 Contact (Robinson Nugent)	61296	CA-11-STL-T3WW
-	Socket, SIP, 20 Contact (Robinson Nugent)	61299	CA-20-STL-T3WW
-	Socket, SIP, 12 Contact (Robinson Nugent)	61297	
-	Socket, SIP, 14 Contact (Robinson Nugent)	61298	

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TABLE 6-14. PARTS LIST LCD-LED CIRCUIT CARD ASSEMBLY

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
	LCD-LED Circuit Card Assembly	09501	
DS1-DS8, DS17-DS32	LED (Data Display Products SP811211-Y)	09806	
DS9-DS16	Not Used		
E1, E2	Terminal	70028	
R1-R4, R6, R7	Resistor, Fixed, Comp., 180 ohm, ½ WVDC, 5%	10945	
R5, R8	Resistor, Not Used		
W1	Cable Assembly	08320	
-	Printed Circuit Card	09502	

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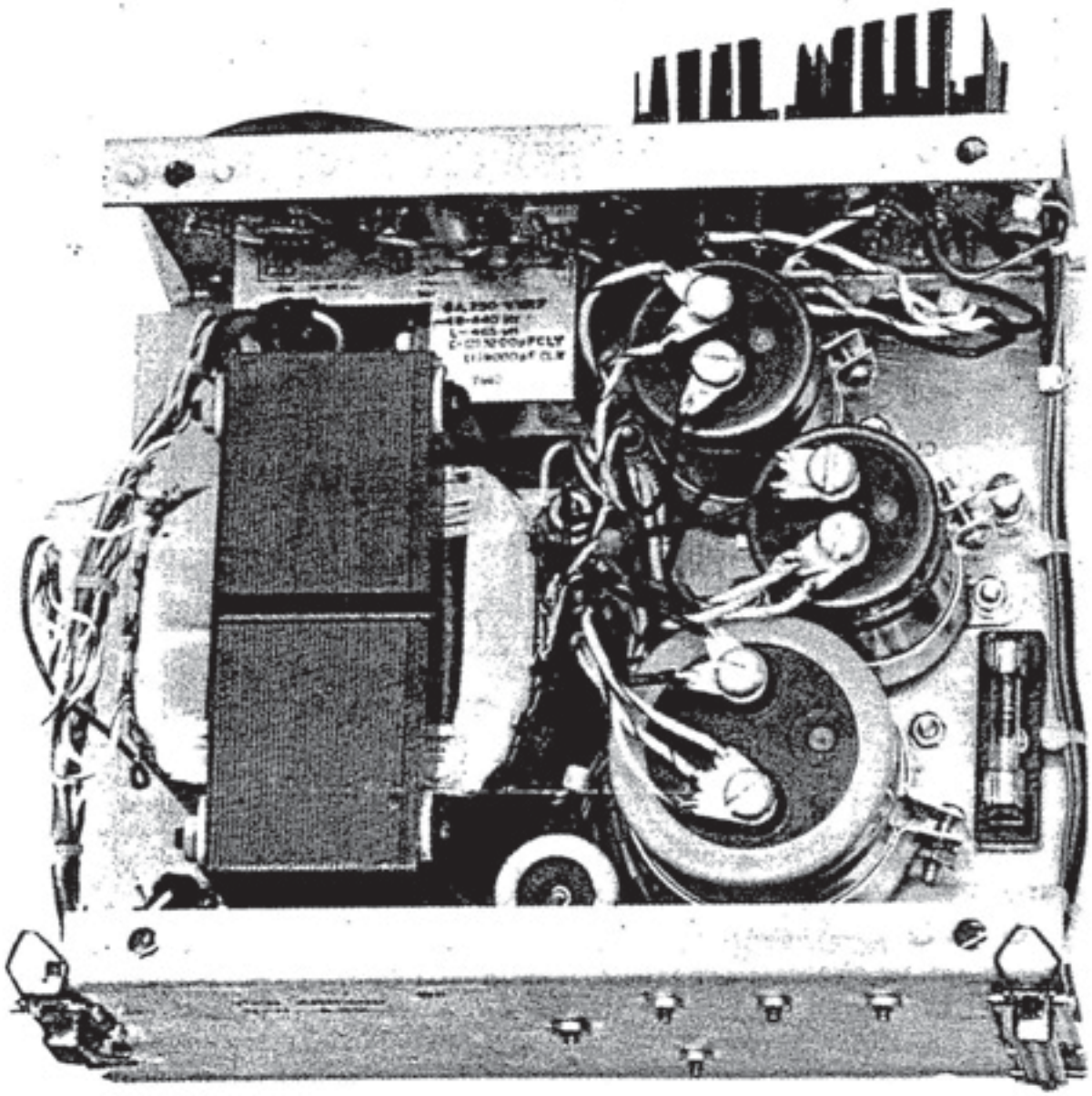

Figure 6-26. Power Supply Assembly, A10, Top View

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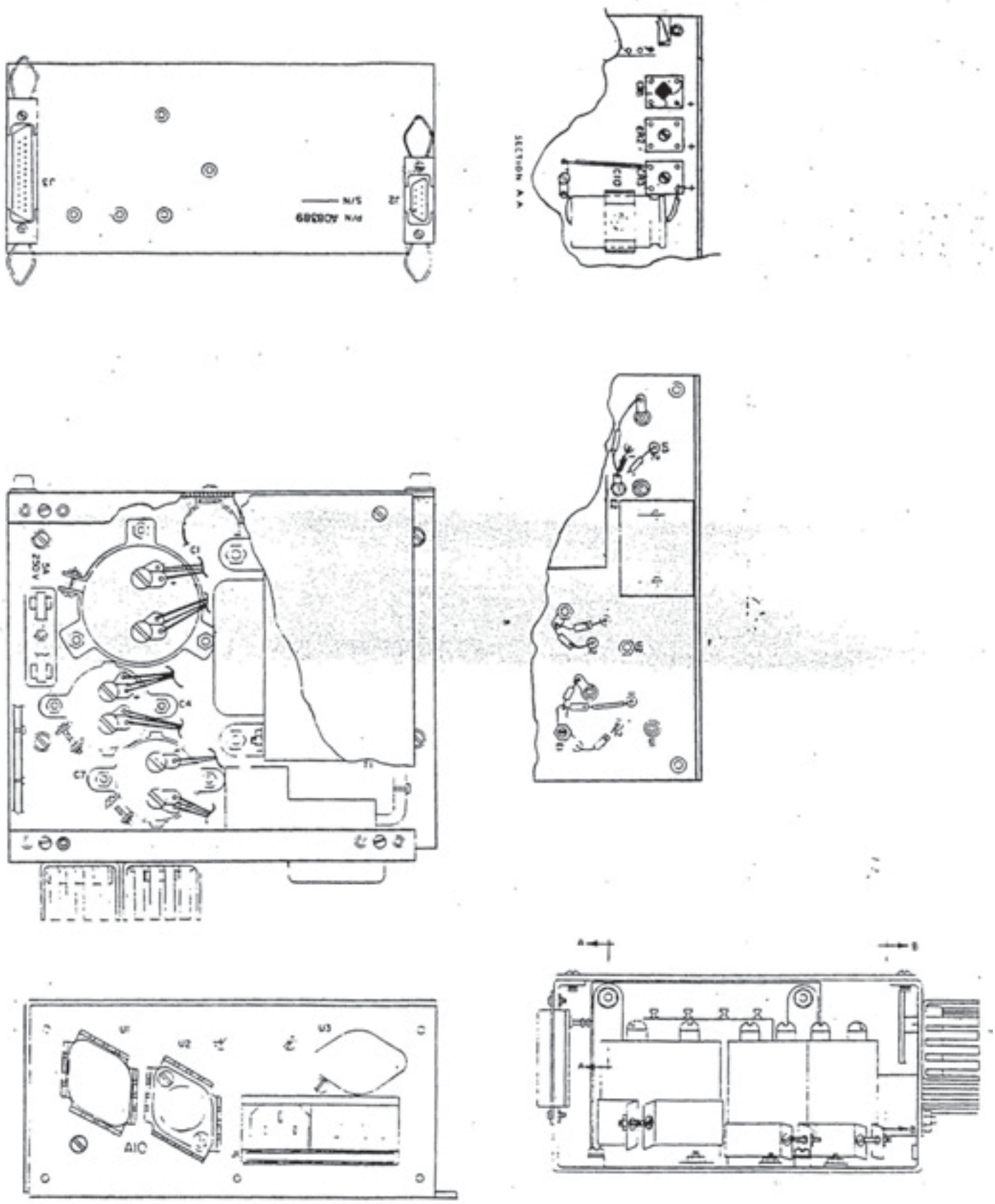

Figure 6-27. Component Location Diagram, A10

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TABLE 6-15. PARTS LIST, POWER SUPPLY MODULE ASSEMBLY, A10

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A10	Power Supply Assembly	08389	
A10A2	+20V Reg. Ckt. Card Assy. (see Table 6-16)	08593	
C1	Capacitor, Electrolytic, 12500 uF, 25 WVDC, -10 +75% (Electra)	24063	3186EA123U025AMA2
C2, C3, C5, C6, C8	Capacitor, Tantalum, 1 uF, 35 WVDC, ±20% (Union Carbide)	25068	T310A105M035AS
C4, C7	Capacitor, Electrolytic, 5200 uF, 40 WVDC, -10 +75% (Electra)	24070	3186BA522U040AM
C9	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25069	T310B685M035AS
C10	Capacitor, Electroyltic, 1200 uF, 50 WVDC, -10 +75% (Electra)	24071	3050HJ122U050JM
C11	Capacitor, Ceramic, 0.22 uF, 50 WVDC, ±20%	21742	M39014/02-1356
CR1	Diode, Rectifier (Varo)	35561	VH148X
CR2, CR3	Diode, Rectifier (Varo)	35560	VS148X
F1	Fuse, 1 amp., Slo-Blo, 125V	40012	F02B250V1-2A
J1	Connector, Power Input, Filter and Fuse (Components Corp.)	61236	6J4
J2	Connector, ac, Switched Power	61166	M24308/2-1
J3	Power Supply Connector Assembly	08516-1	
R1	Resistor, Metal Film, 33 ohms, ±2%, 1/4W	12161-330	RLR07C330GR
T1	Transformer, Power	08517	
U1	IC, Regulator, +5 V, 5 amp.	36627	UA78H05KC
U2	IC, Regulator, +15 V, 1 amp. (Fairchild)	36755	UA7815KC
U3	IC, Regulator, -15 V, 1 amp.	36756	LM7915C
-	Fuse, 1/2 amp., Slo-Blo, 250V, 3AG	40028	F02B250V1-1A
-	Fuseholder, Clip Type, Spare for 220 V (Littlefuse)	40503	350244
-	Wiring Harness No. 1 Assembly	08513	
-	Wiring Harness No. 2 Assembly	08515	

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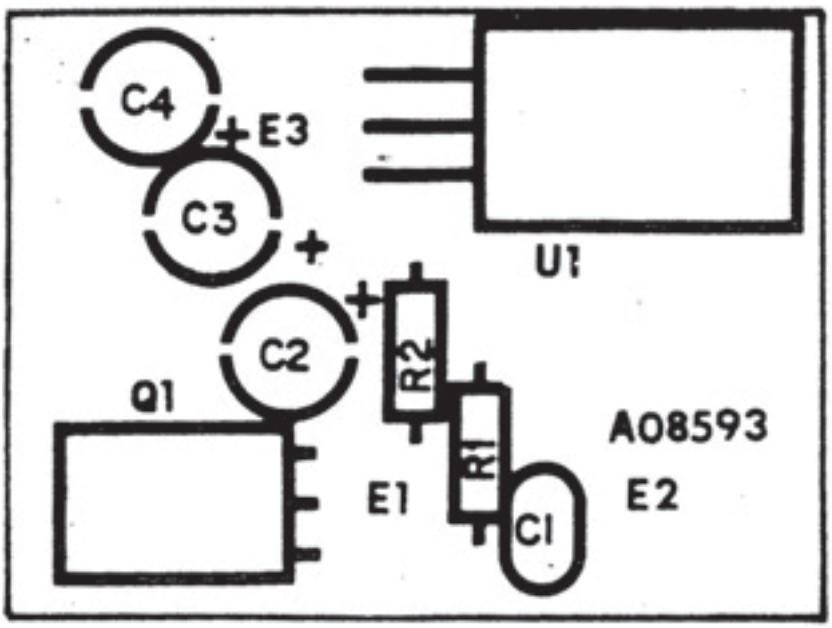

Figure 6-28. Component Location Diagram, A10A2

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TABLE 6-16. PARTS LIST, 20 VOLT REGULATOR ASSEMBLY, A10A2

Reference Designation	Description	RACAL Number	Manufacturer/ MIL Part No.
A10A2	20 Volt Regulator Circuit Card Assembly	08593	
C1	Capacitor, Ceramic, 0.01 uF, 50 WVDC, ±20% (Erie)	21733	8121-050-651-103M
C2, C4	Capacitor, Tantalum, 6.8 uF, 35 WVDC, ±20% (Union Carbide)	25060-685	T362A685M035AS
C3	Capacitor, Tantalum, 1 uF, 50 WVDC, ±20% (Union Carbide)	25078-105	T362A105M035AS
Q1	Transistor, Voltage Regulator (Motorola)	32519	MJE800
R1	Resistor, Film, 4.7K, ±2%, 1/4W	12161-472	RLR07C472GR
R2	Resistor, Film, 47K, ±2%, 1/4W	12161-473	RLR07C473GR
U1	IC, +20 Volt DC Regulator (Motorola)	36819	MC78M20CT

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SECTION VII
SCHEMATIC DIAGRAMS

7.1 INTRODUCTION

Section VII contains circuit diagrams and interconnection diagrams applicable to the RA6790/GM HF Receiver. A listing of all diagrams, showing Figure number and Page number for each, is shown below for quick reference to any diagram.

Figure No.	Title	Page
7-1	Schematic Diagram, RF Low Pass Filter, A1	7-3
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7-5	Schematic Diagram, ISB, A5 (Optional) (Sheet 1)	7-21
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7-6	Interconnection Diagram, Microcomputer Assembly, A6	7-25
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7-10	Schematic Diagram, Second LO/BFO Synthesizer A8 (Sheet 1)	7-45
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NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

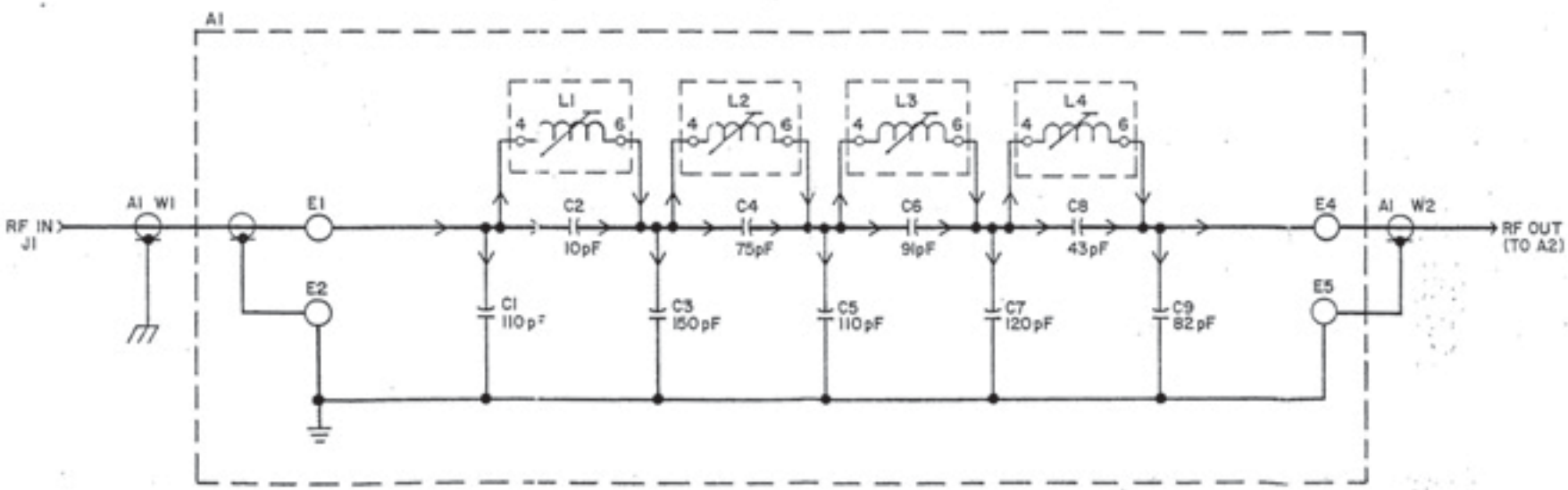

Figure 7-1. Schematic Diagram, RF Low Pass Filter, A1

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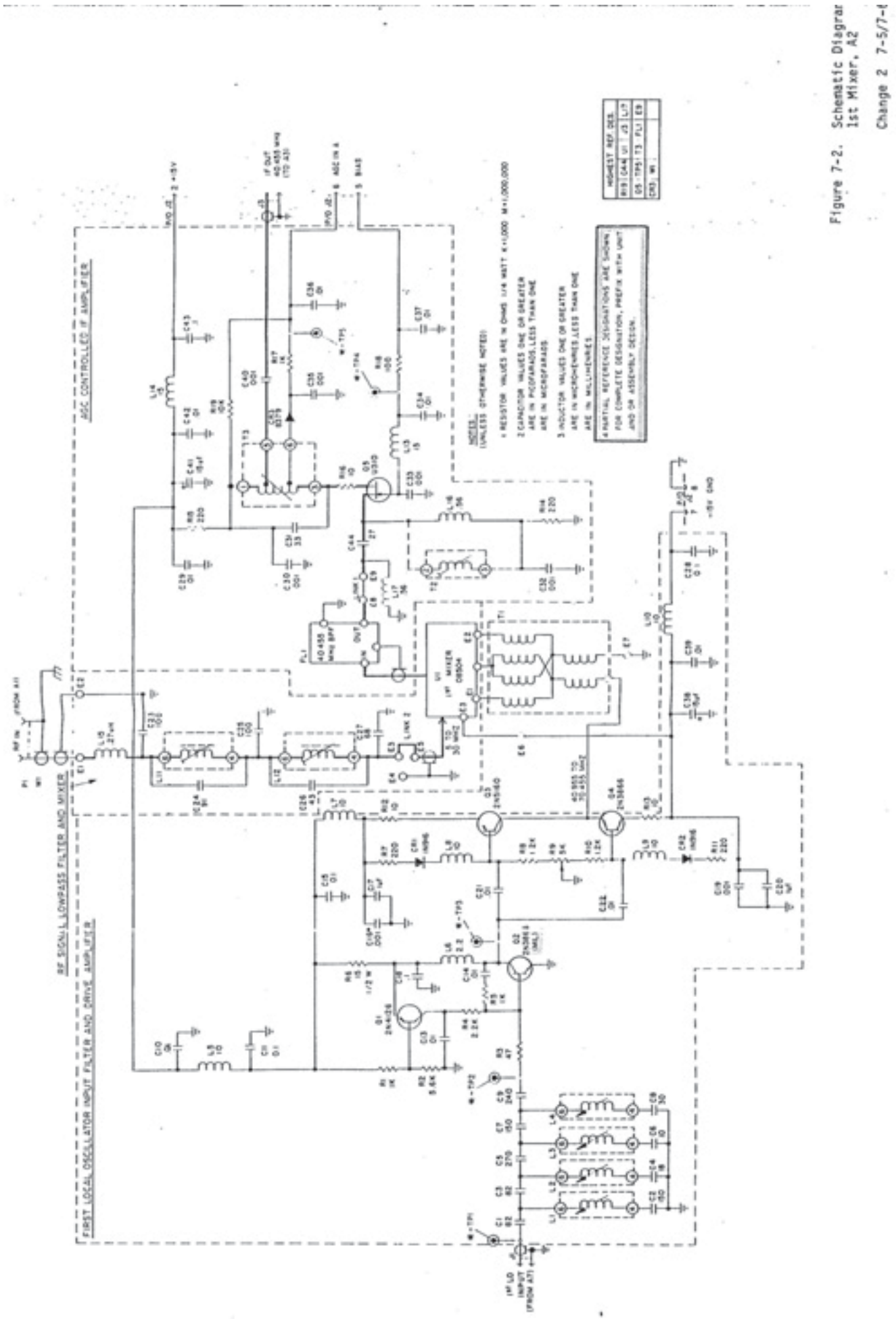

Figure 7-2. Schematic Diagram
1st Mixer, A2

Change 2 7-5/7-6

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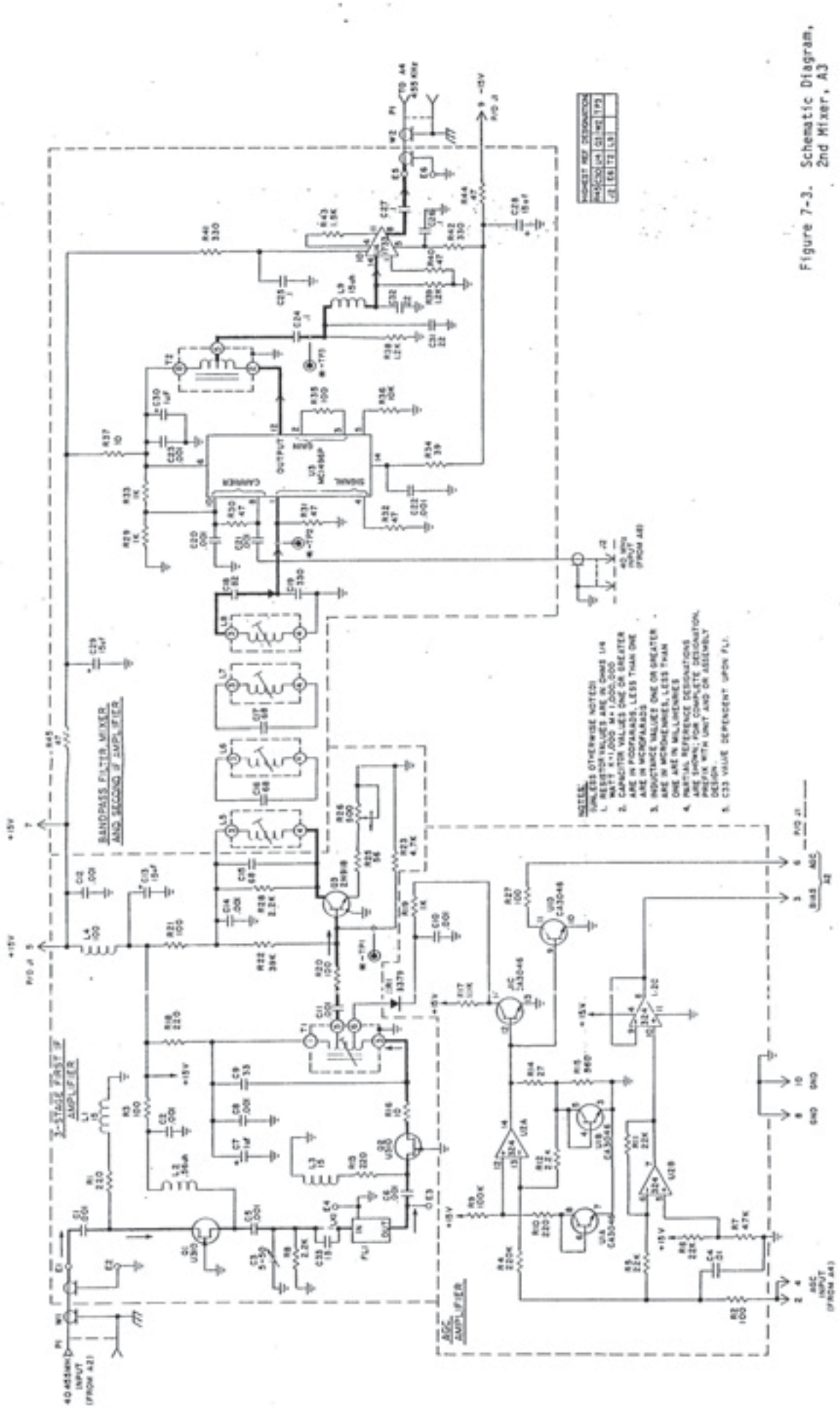

Figure 7-3. Schematic Diagram, 2nd Mixer, A3

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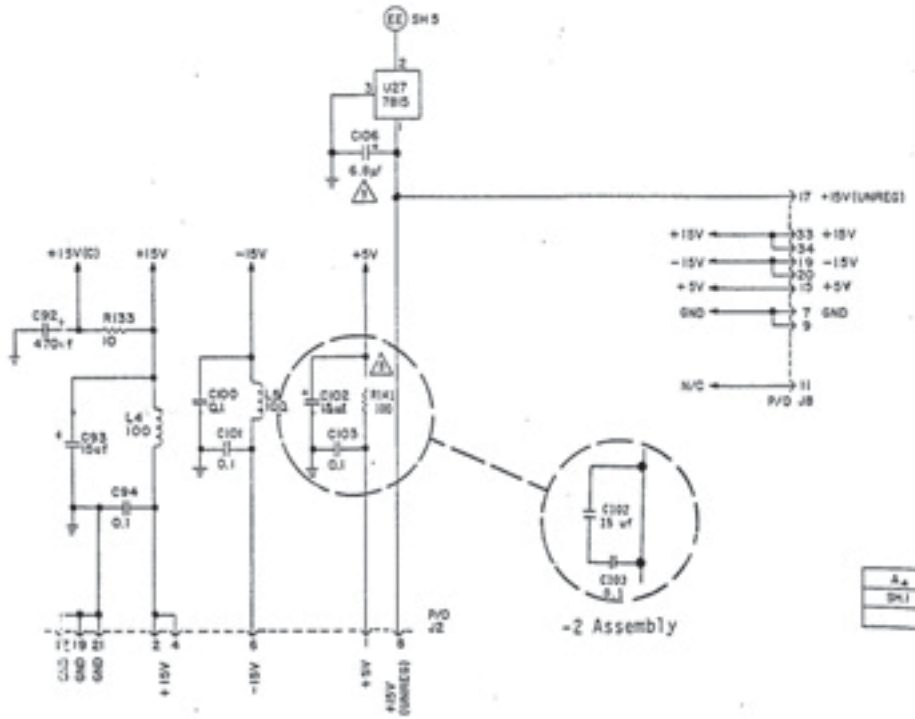
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES LESS THAN ONE ARE IN MILLIHENRIES.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. ▵ = VALUE DEPENDENT ON FILTER COMPLEMENT.
6. FOR ISB OPERATION CONNECT LINK 1 TO ISB.
7. PROVIDE MUTE ONLY IF MUTE MODULE IS INSTALLED.
8. ⚠ R141 IS USED ON -1 ASSEMBLY, AND IS DELETED ON -2 ASSEMBLY, AND REPLACED WITH BUSS WIRE AND SLEEVING.
9. ⚠ C106 IS 68μF FOR -2 ASSEMBLY ONLY.

I.C. NO.	DEVICE	GND	+15V(B)	+15V(C)	-15V
U7	324	11		4	
U14	324	11		4	
U17	324	11		4	
U9	4013	7		14	
U11	4066	7		14	
U12	4066	7		14	
U19	4053	6,7,8		16	
U22	1458			8	4
U24	339	12		3	
U28	1458		8		4
U29	1458	4	8		



A4	A4	A4	A4	A4	A4
SH.1	SH.2	SH.3	SH.4	SH.5	SH.6
REVISION STATUS OF SHEETS					

Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 1 of 6)

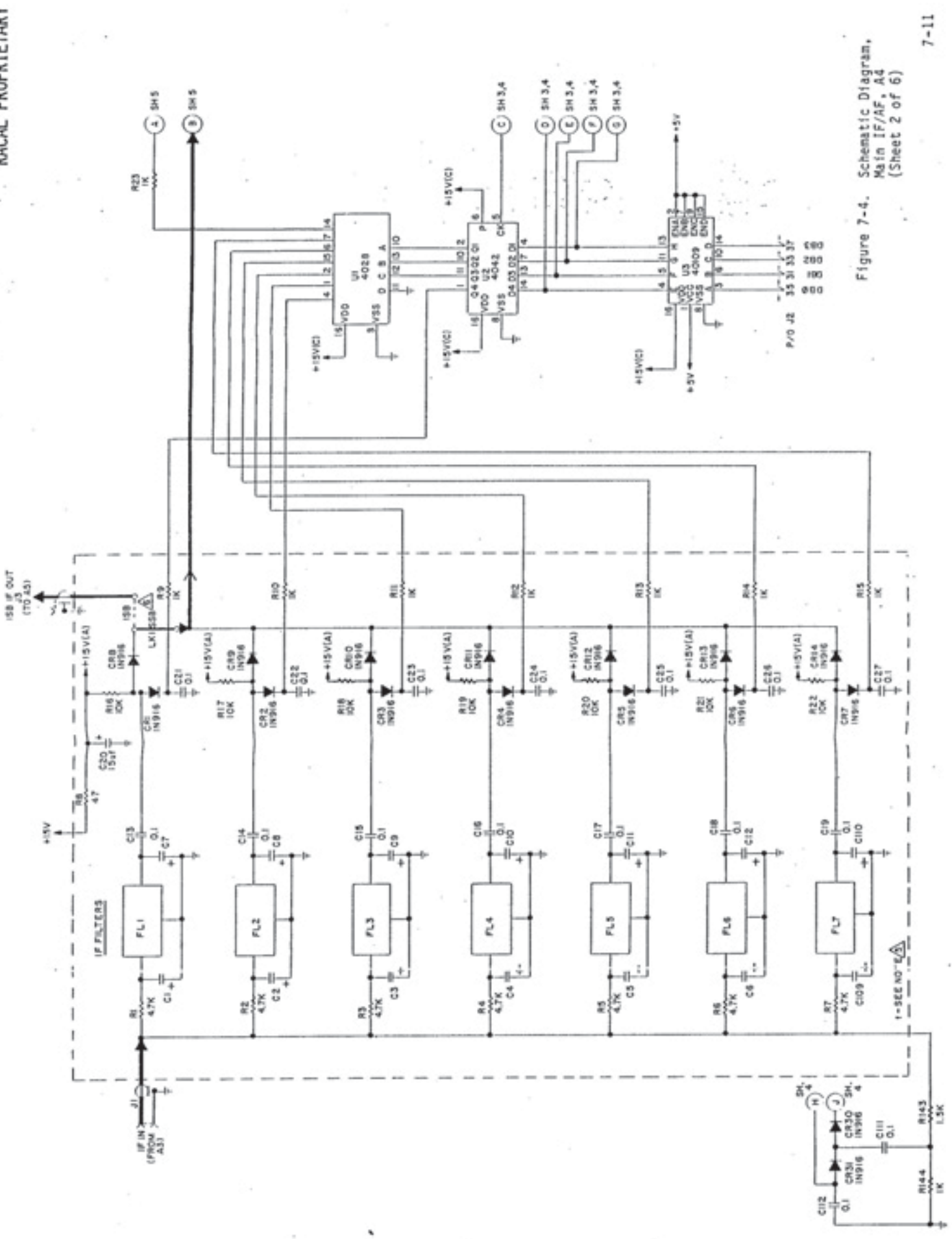


Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 2 of 6)

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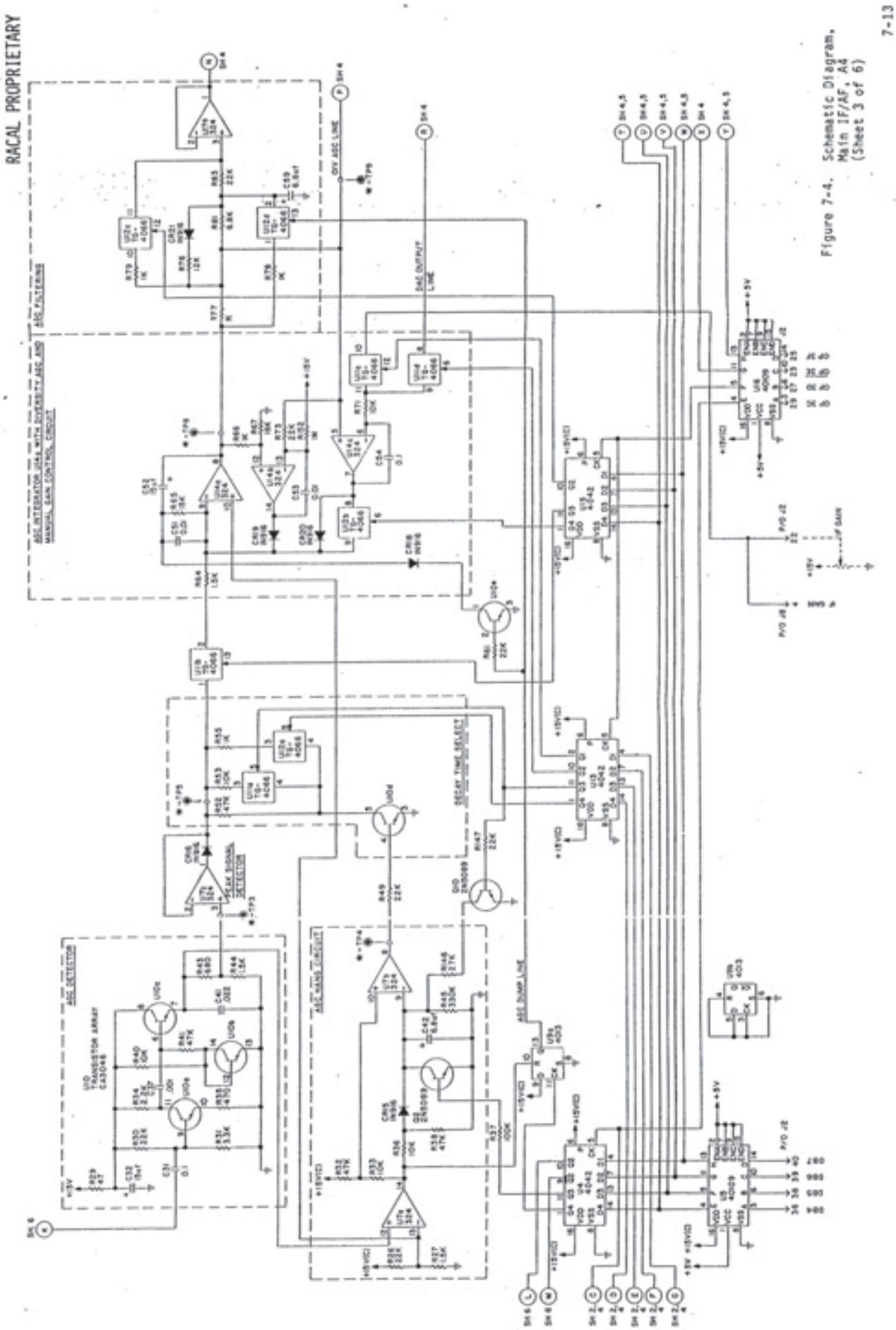

Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 3 of 6)

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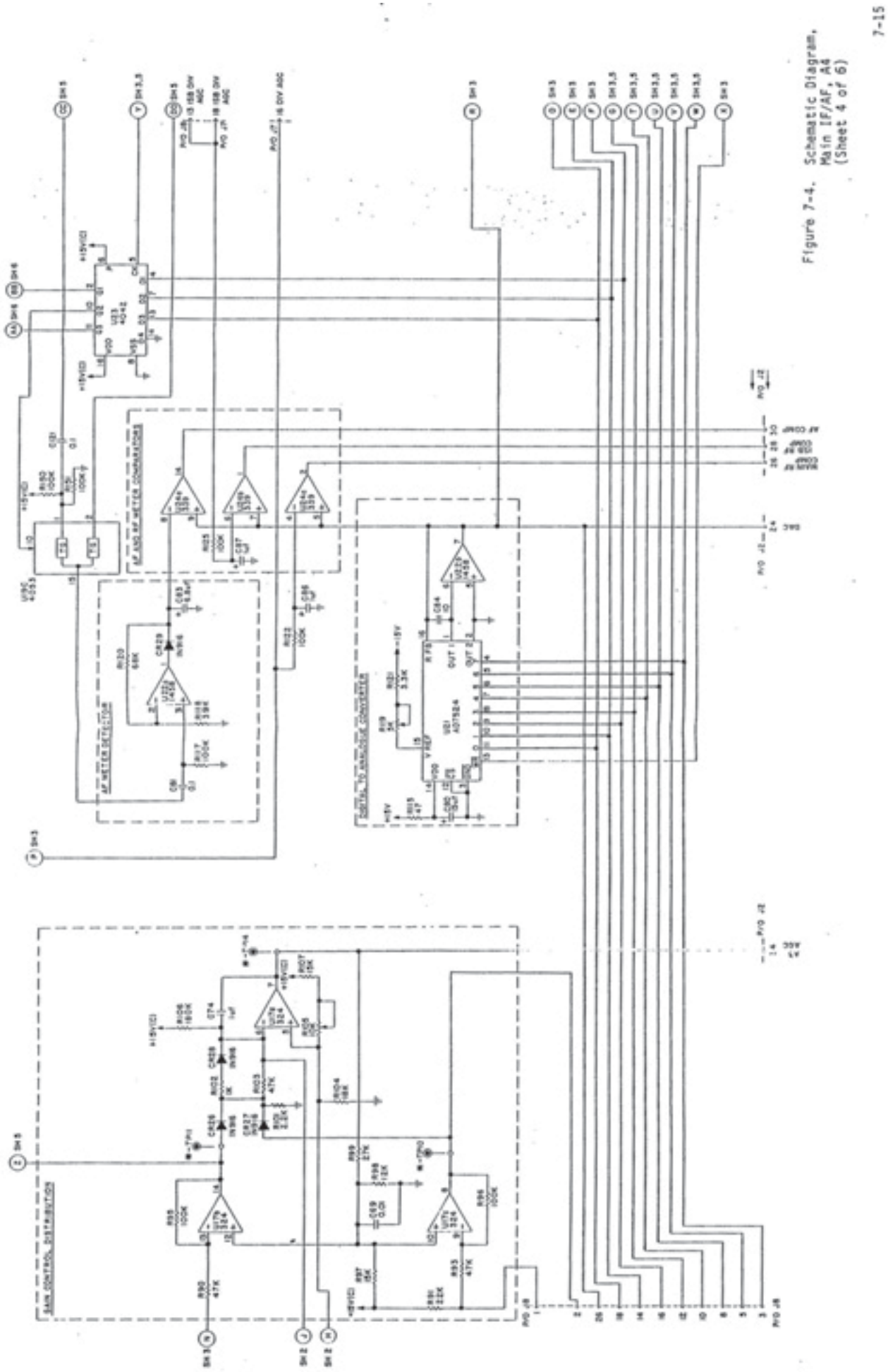

Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 4 of 6)

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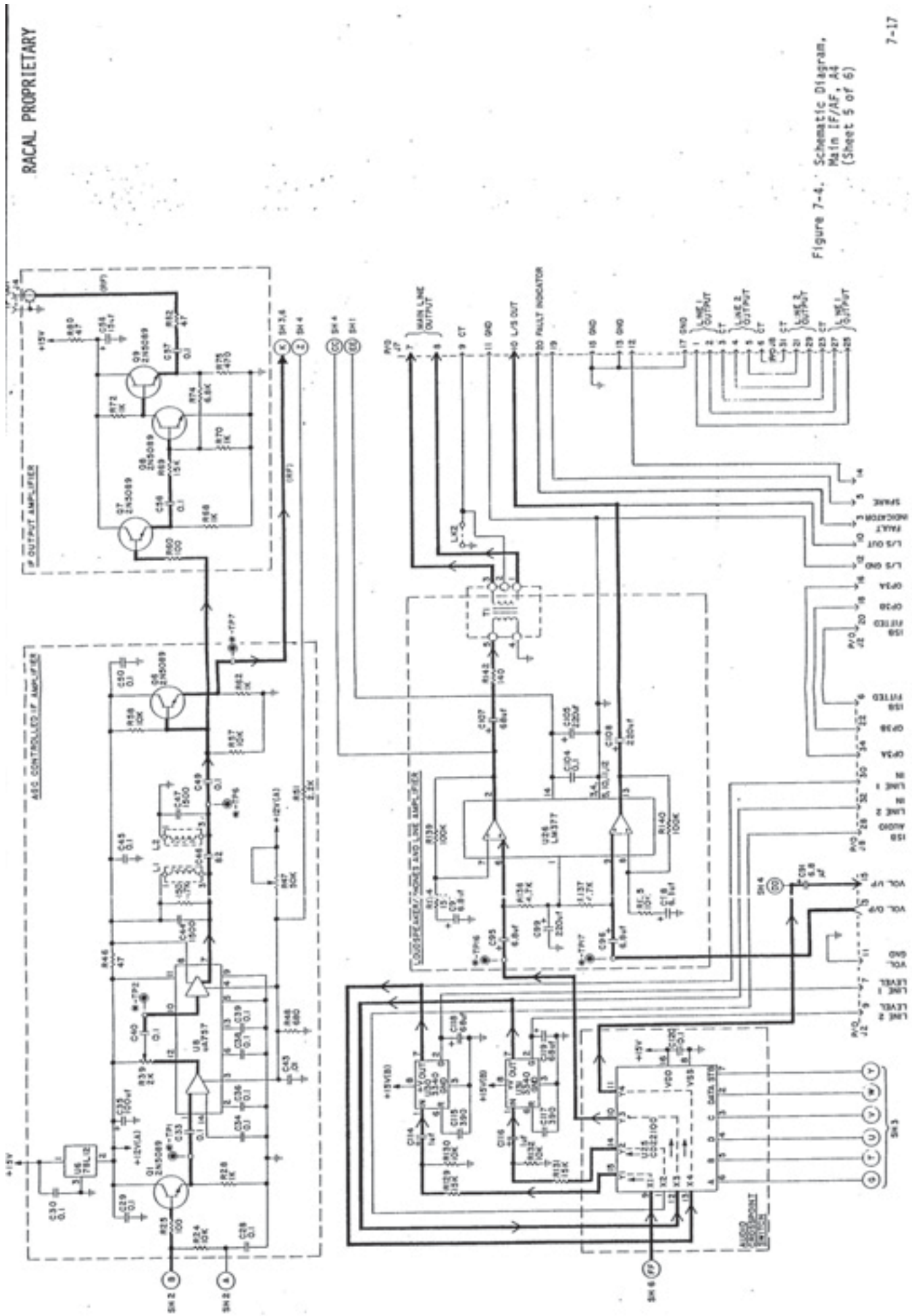
Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 5 of 6)



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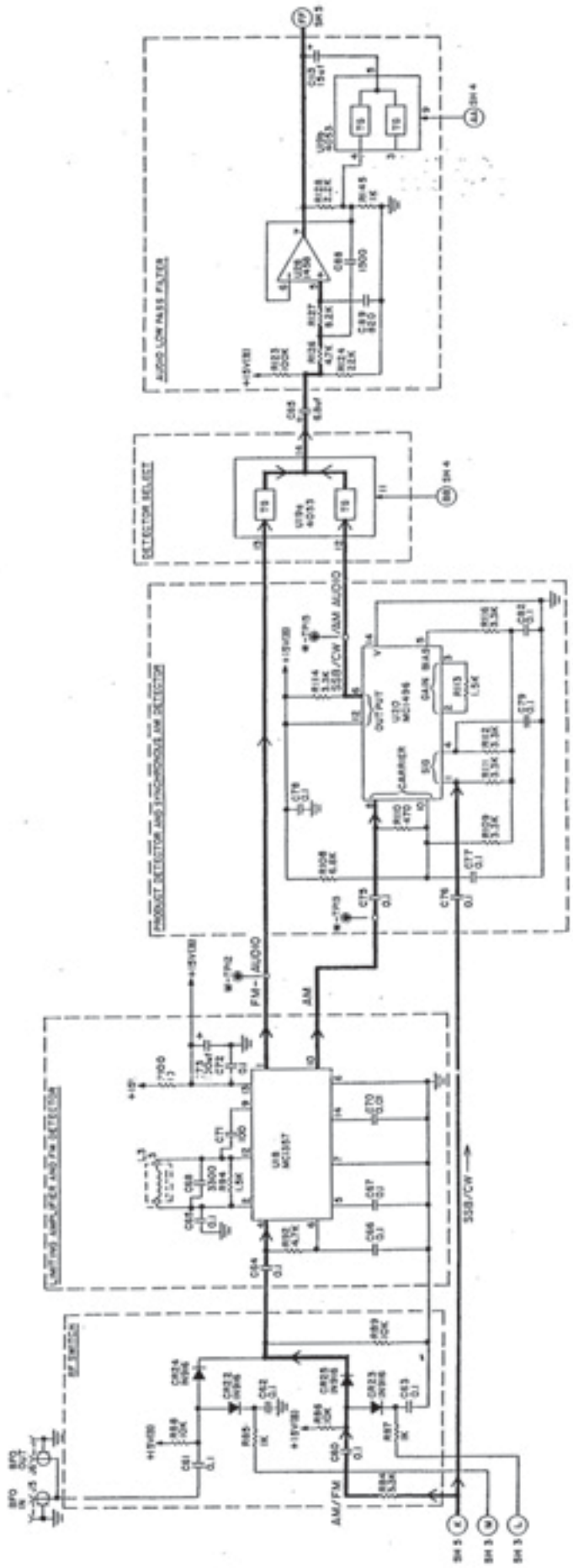

Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 6 of 6)

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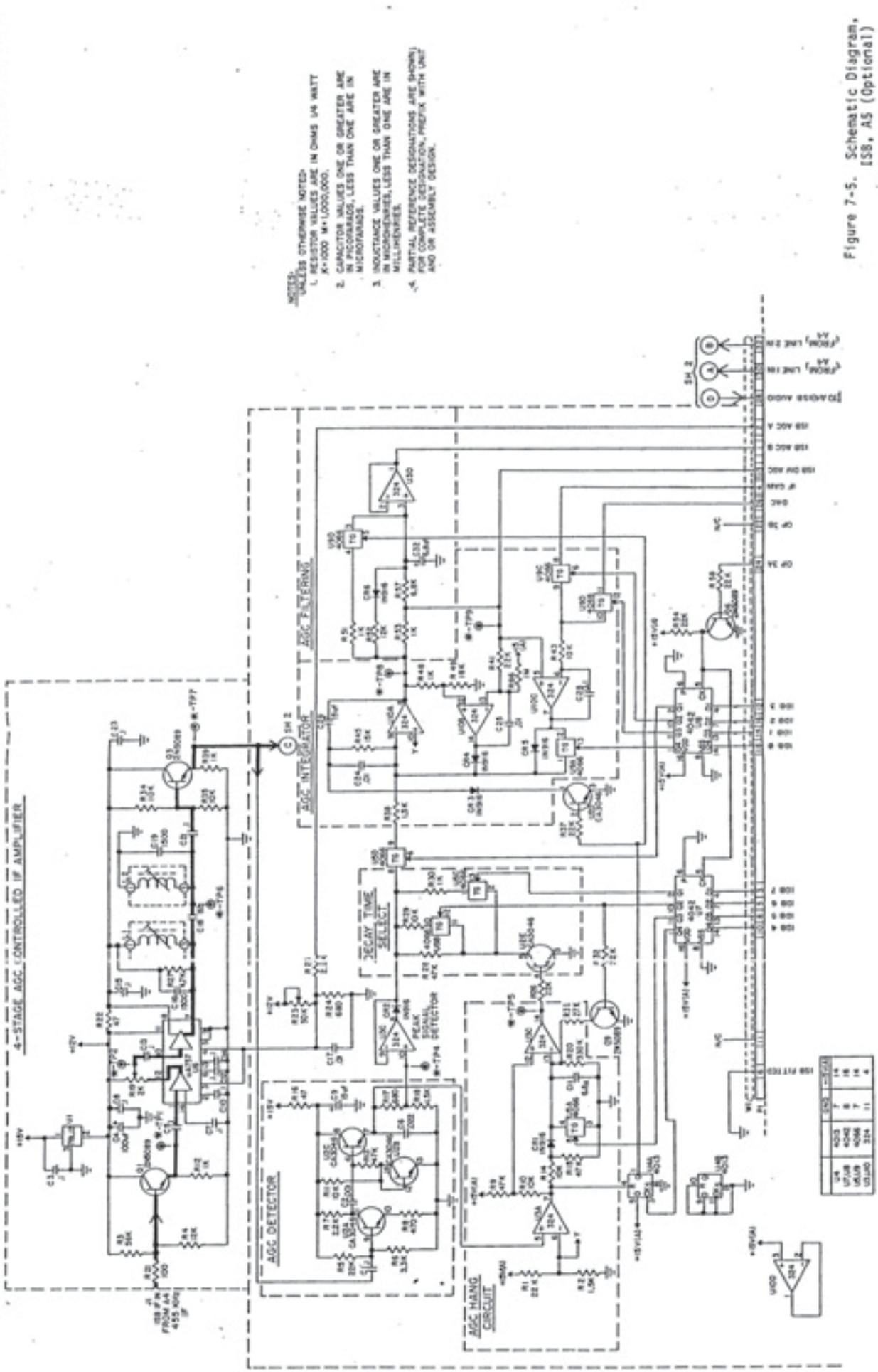

Figure 7-5. Schematic Diagram, ISB, AS (Optional) (Sheet 1 of 2)

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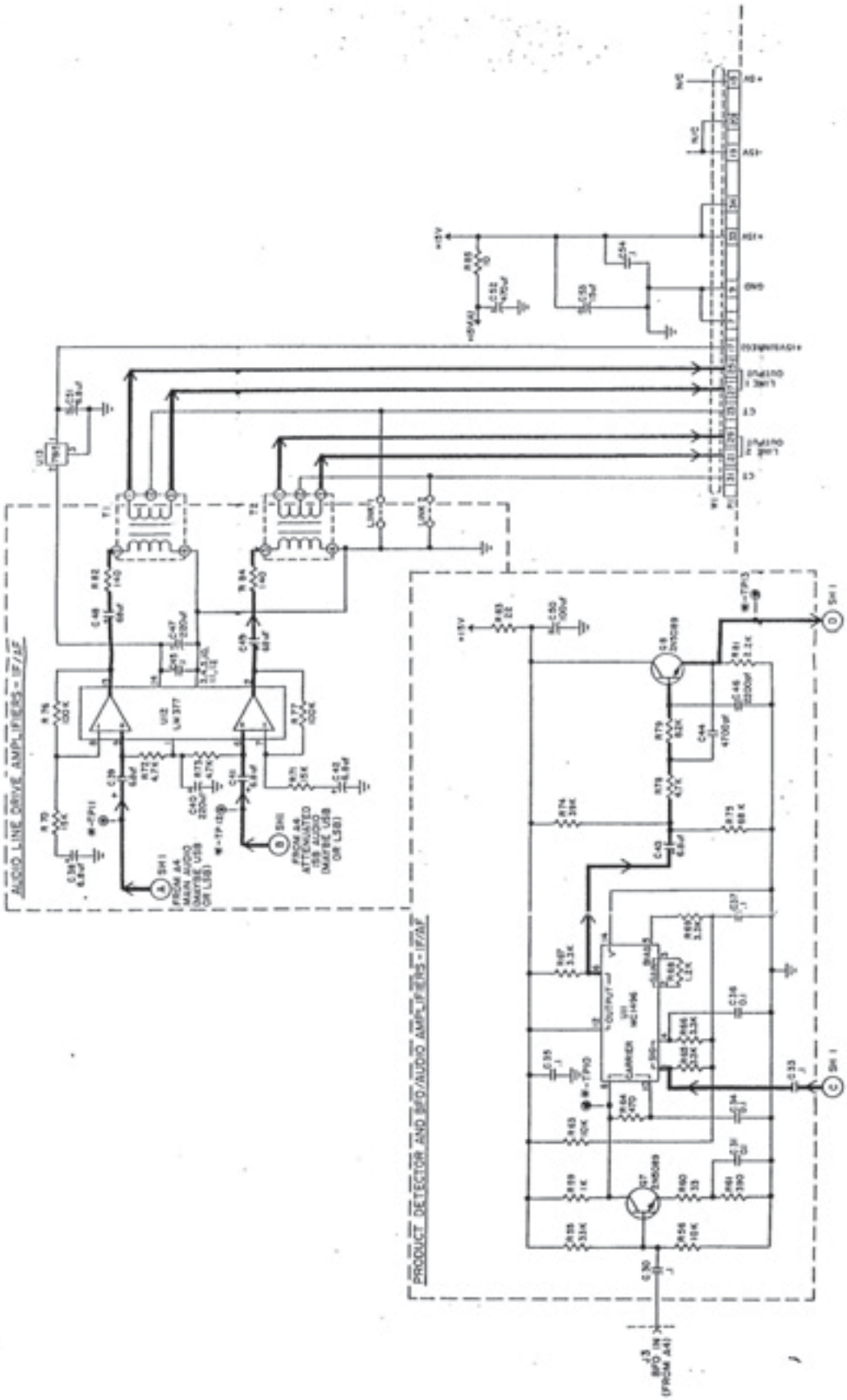

Figure 7-5. Schematic Diagram, ISB, A5 (Optional) (Sheet 2 of 2)

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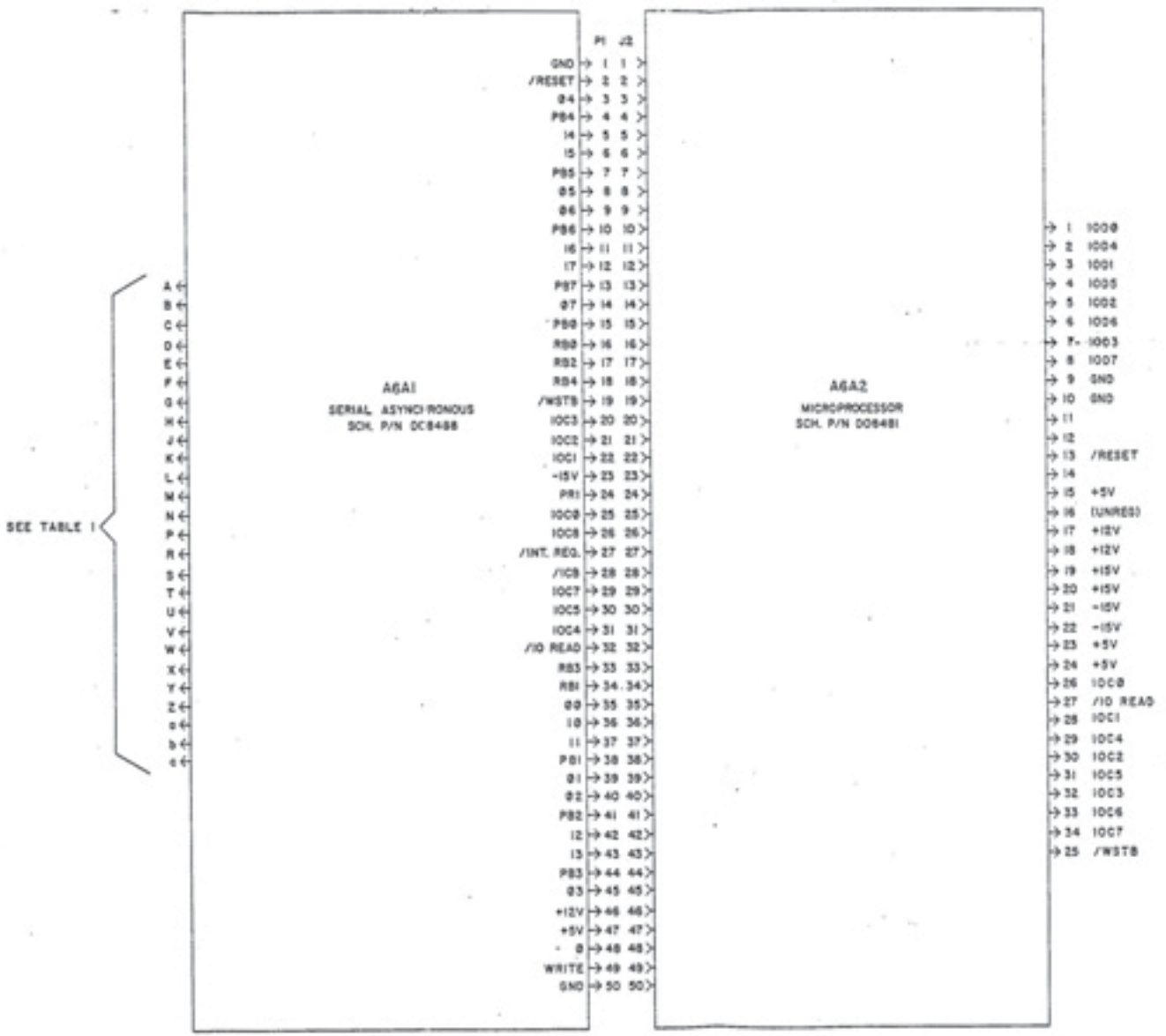

TABLE I

	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND -
F	DATA IN A'
G	DATA IN GND
H	DATA IN B'
J	GND -
K	RECEIVER NUMBER DI-1
L	RECEIVER NUMBER DI-2
M	RECEIVER NUMBER DI-4
N	RECEIVER NUMBER DI-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/ PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

Figure 7-6. Schematic Diagram, Microcomputer Assembly, A6

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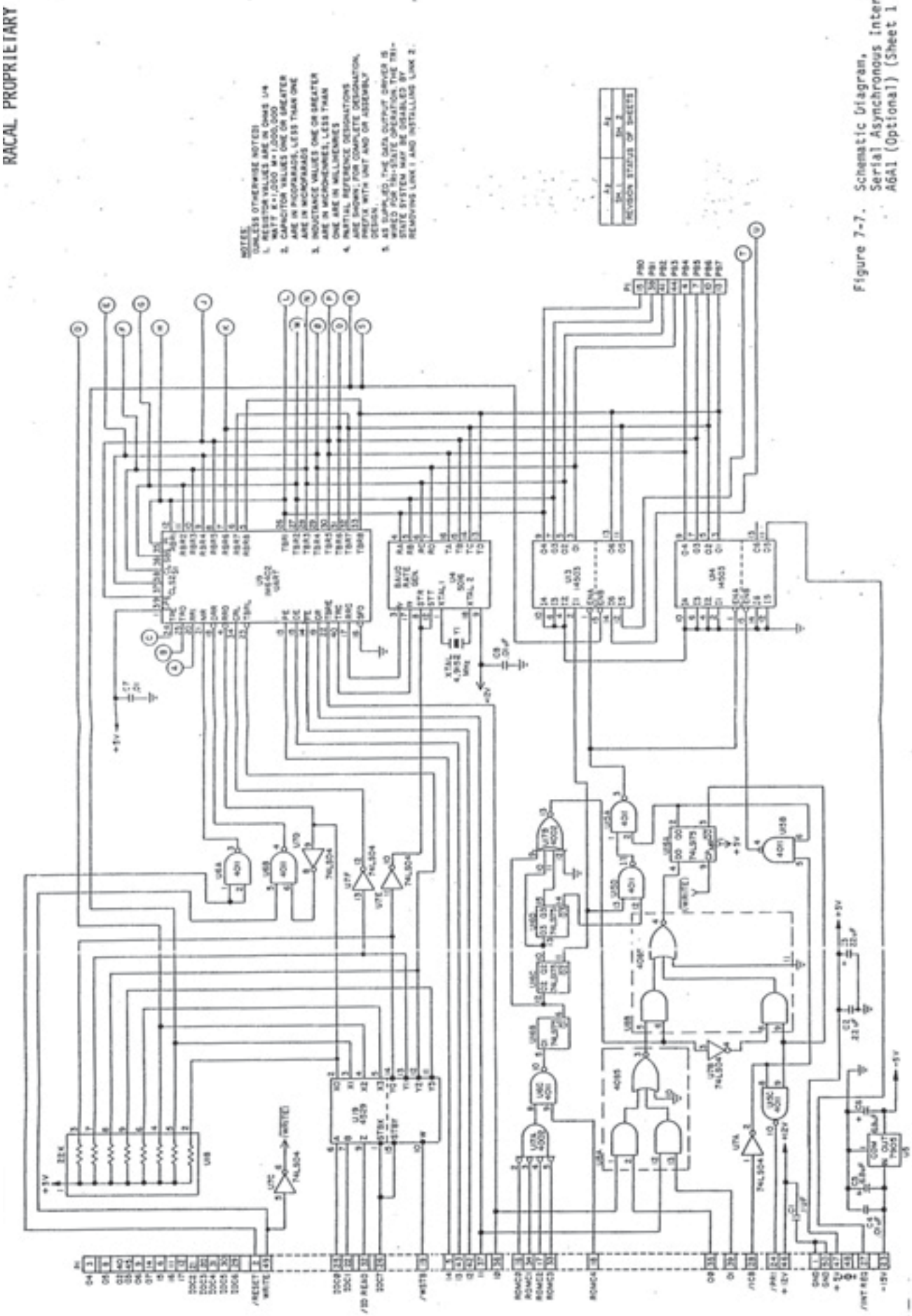

Figure 7-7. Schematic Diagram, Serial Asynchronous Interface, A6A1 (Optional) (Sheet 1 of 2)

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Figure 7-7. Schematic Diagram, Serial Asynchronous Interface, A6A1 (Optional) (Sheet 2 of 2)

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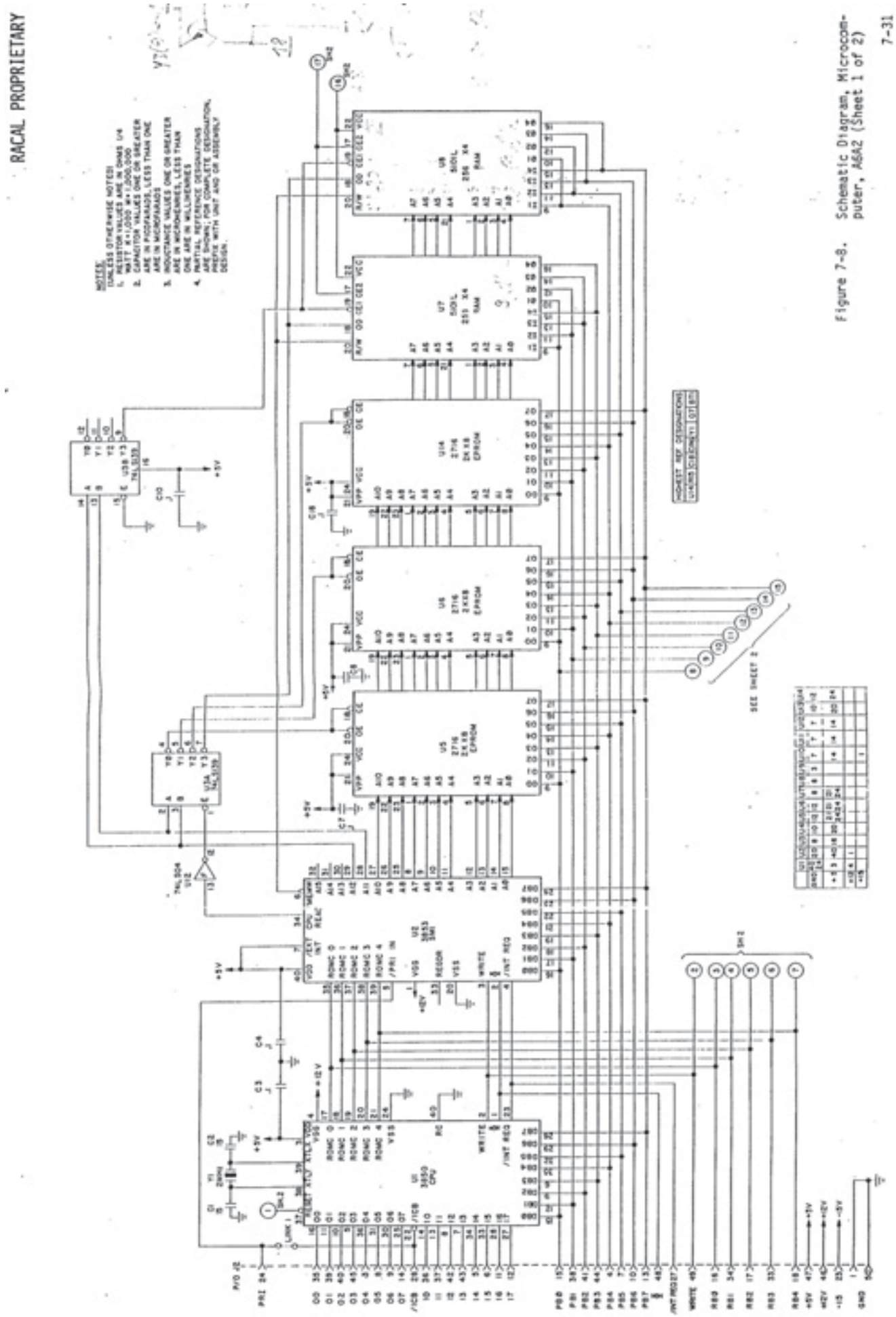

Figure 7-8. Schematic Diagram, Microcomputer, A6A2 (Sheet 1 of 2)

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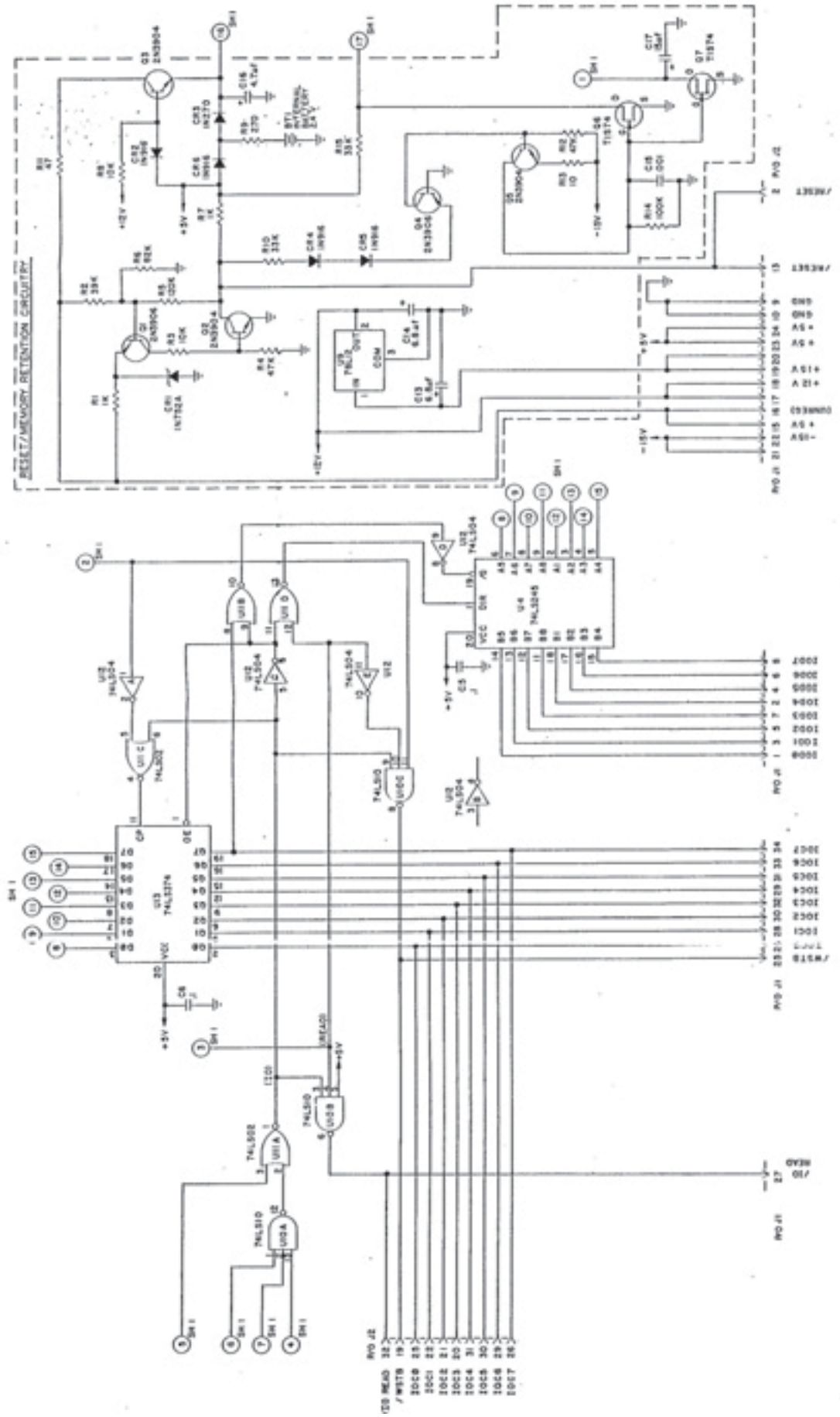

Figure 7-8. Schematic Diagram, Microcomputer, A6A2 (Sheet 2 of 2)

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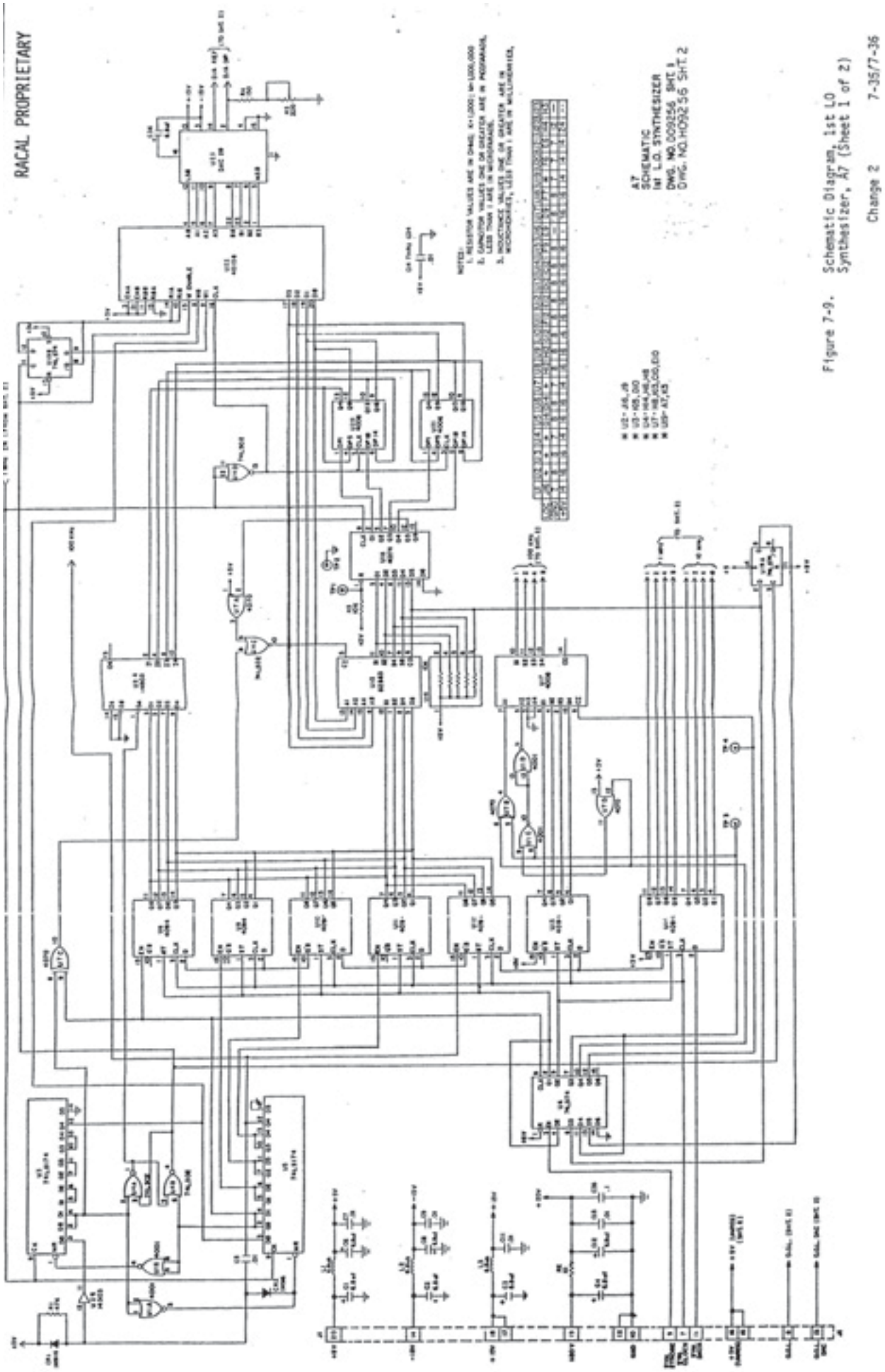

Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 1 of 2)

Change 2 7-35/7-36

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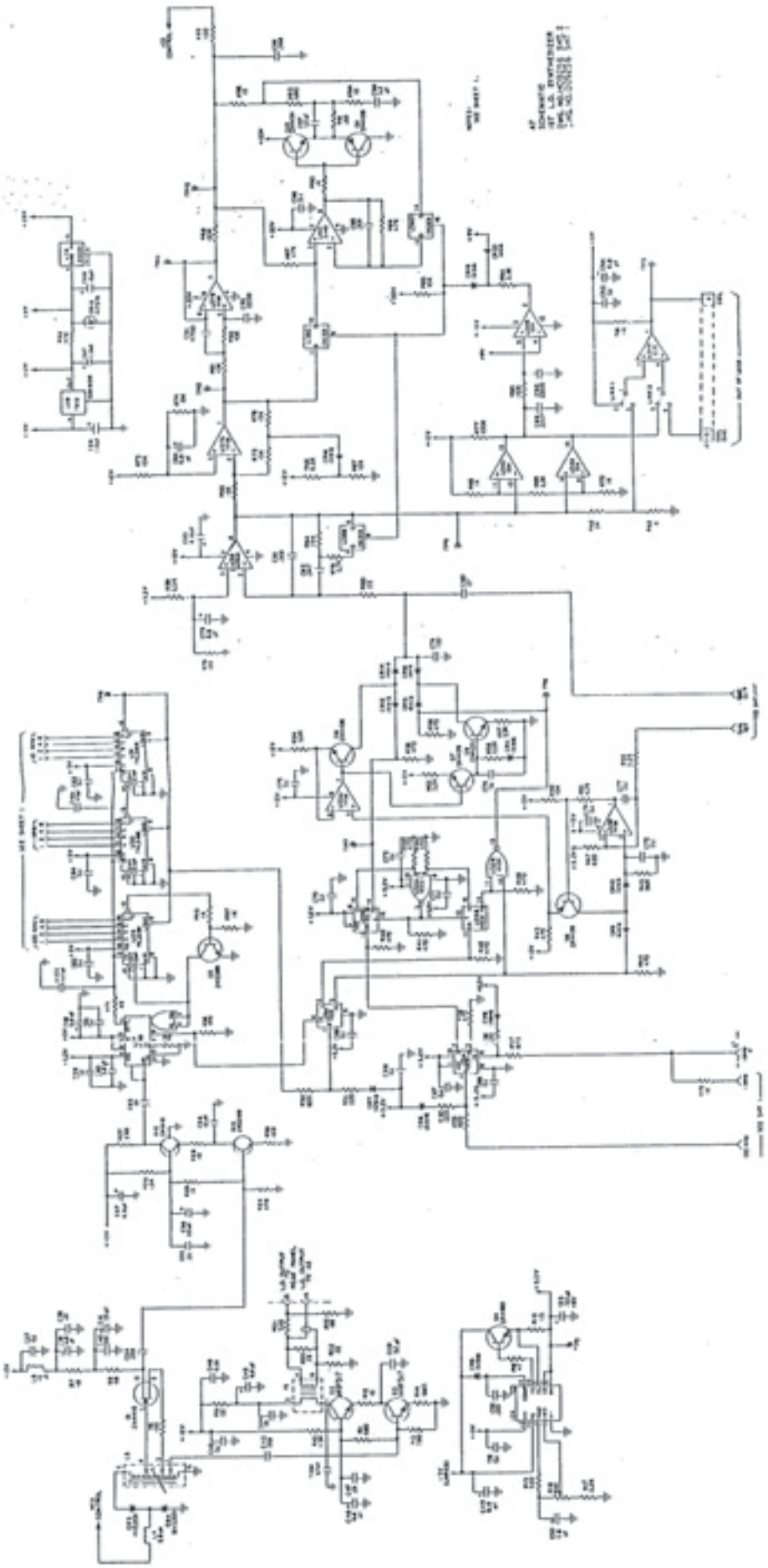

Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 2 of 5)

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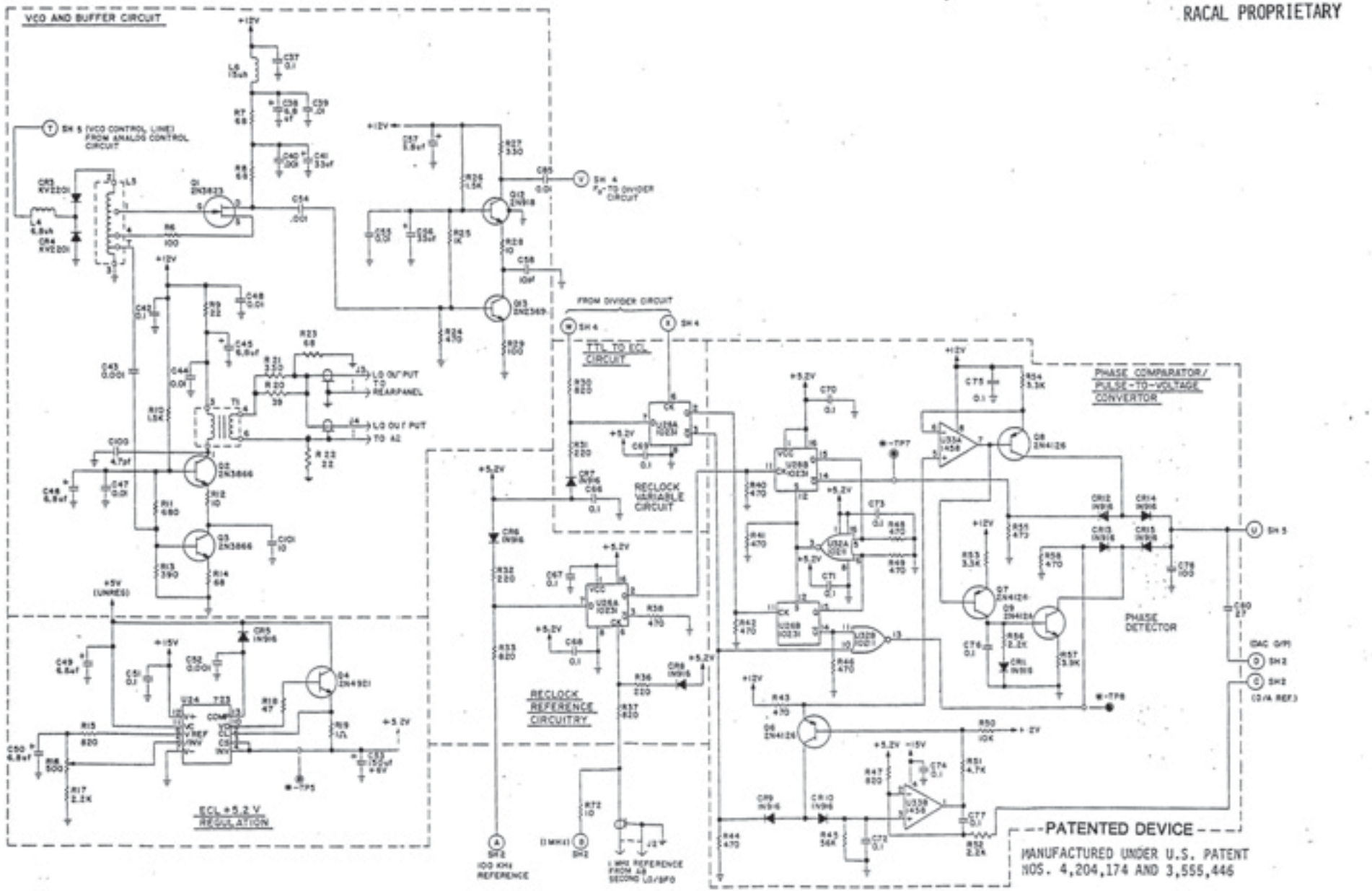

Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 3 of 5)

7-39/7-40

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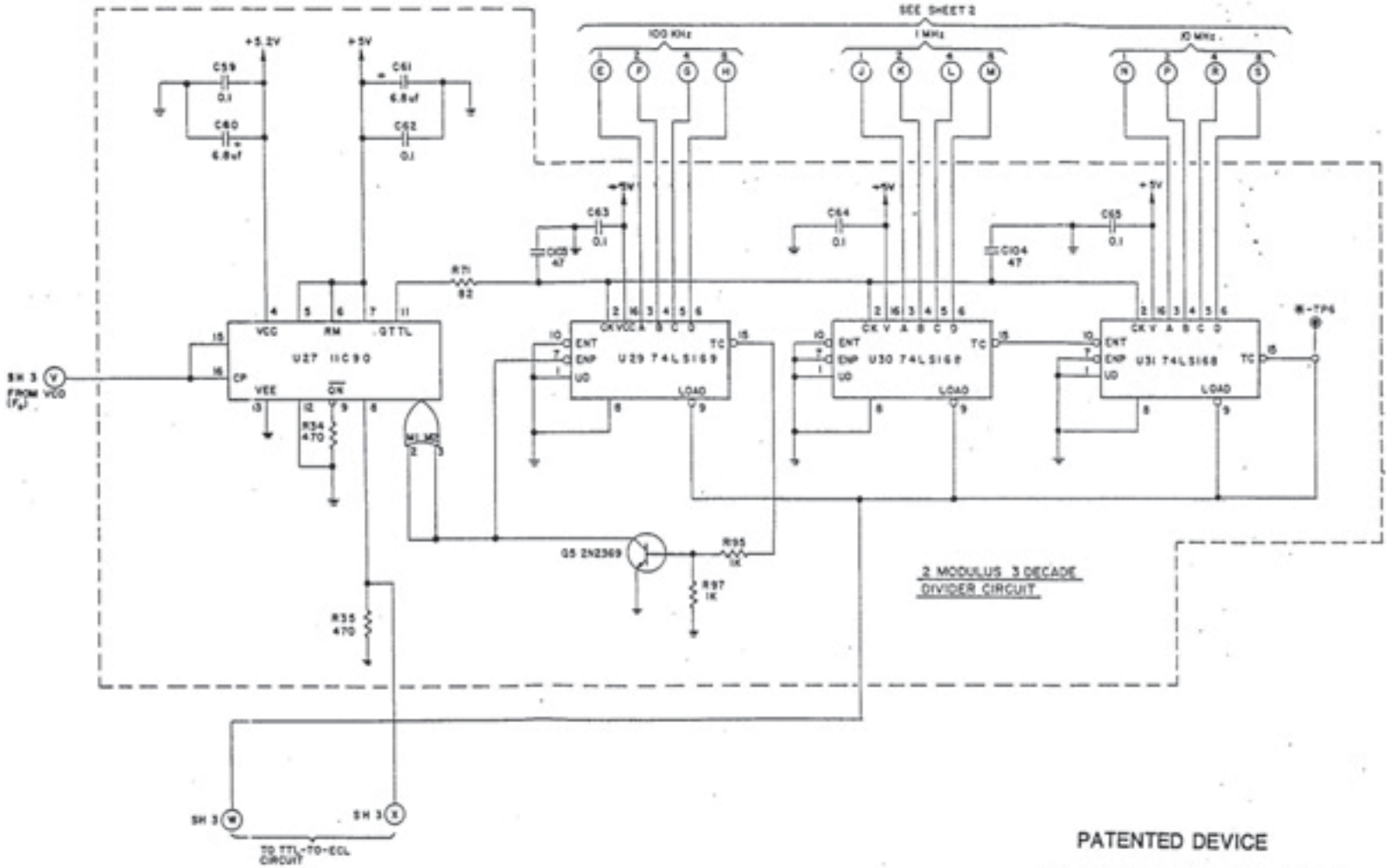
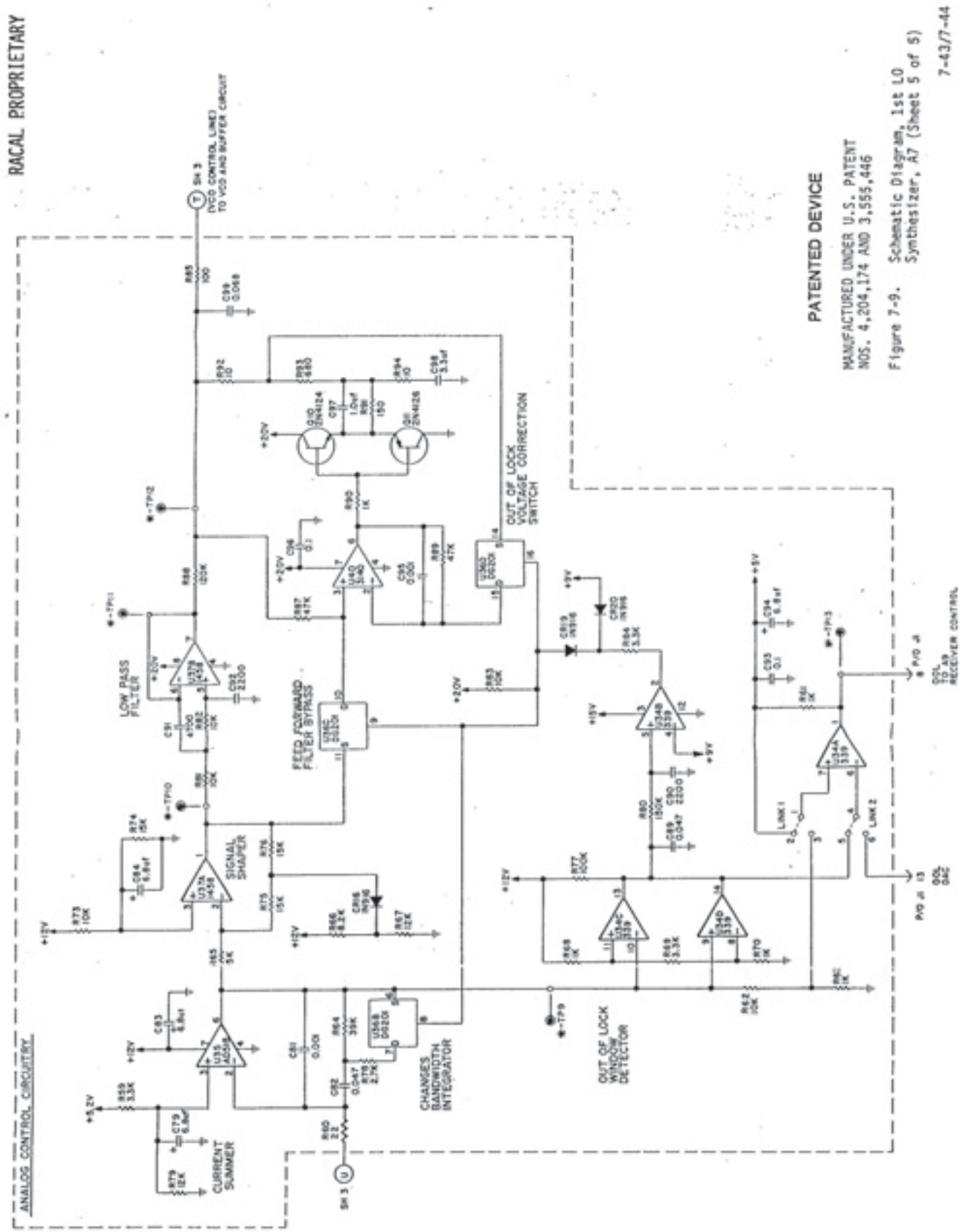


PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT
NOS. 4,204,174 AND 3,555,446

Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 4 of 5)



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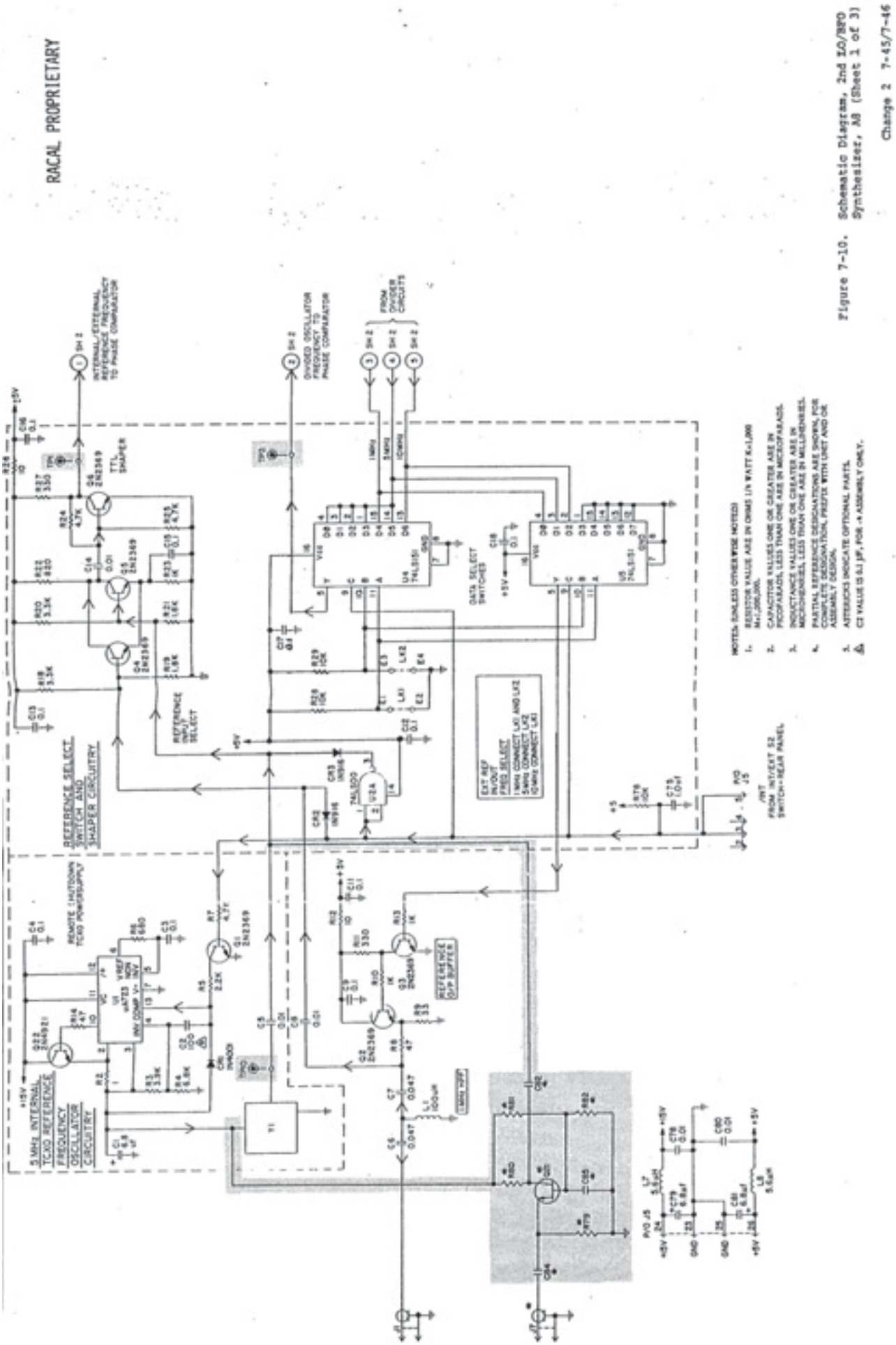

Figure 7-10. Schematic Diagram, 2nd IO/BFO Synthesizer, A8 (Sheet 1 of 3)

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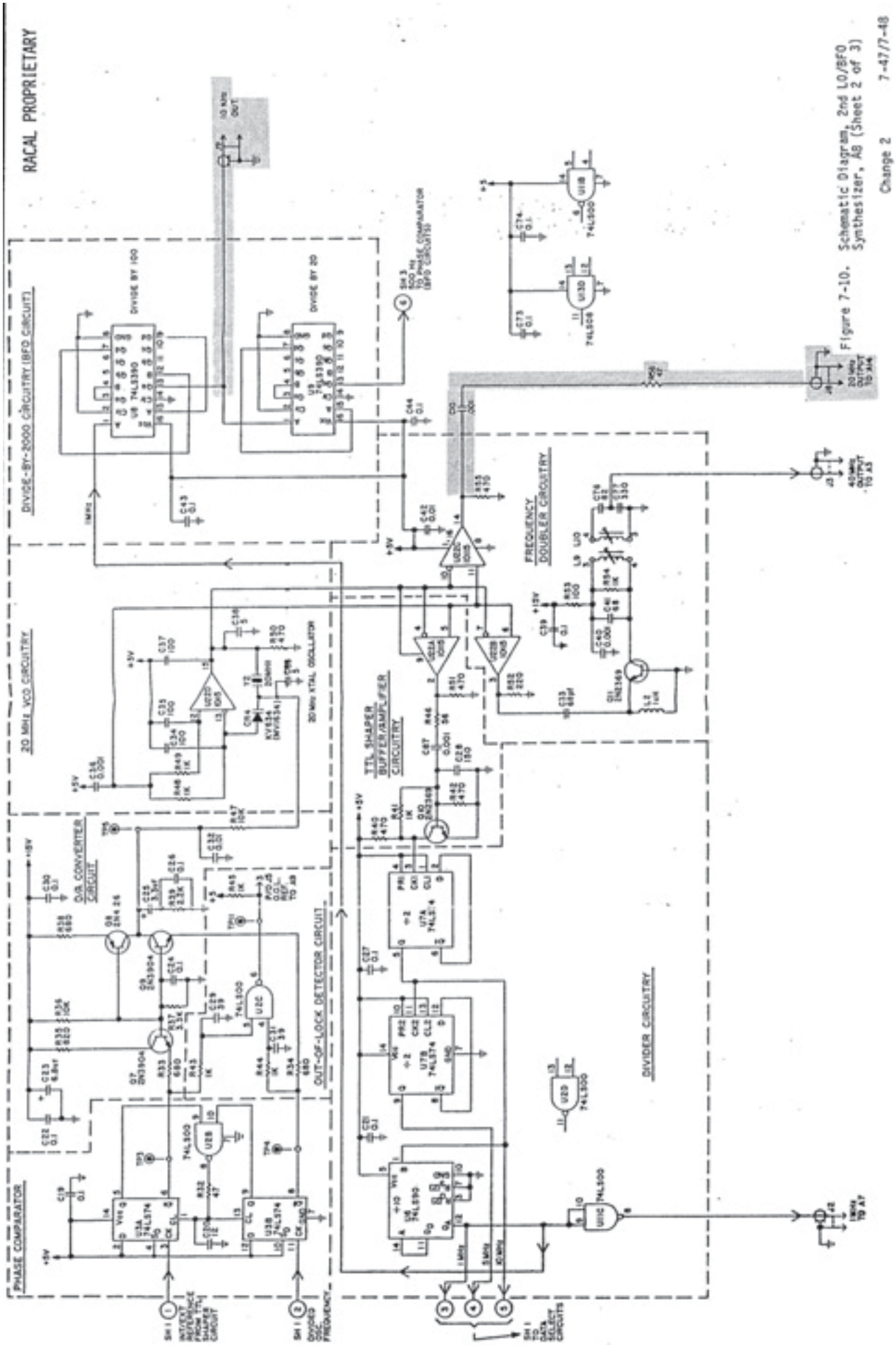

Figure 7-10. Schematic Diagram, 2nd LO/BFO Synthesizer, A8 (Sheet 2 of 3)

Change 2 7-47/7-48

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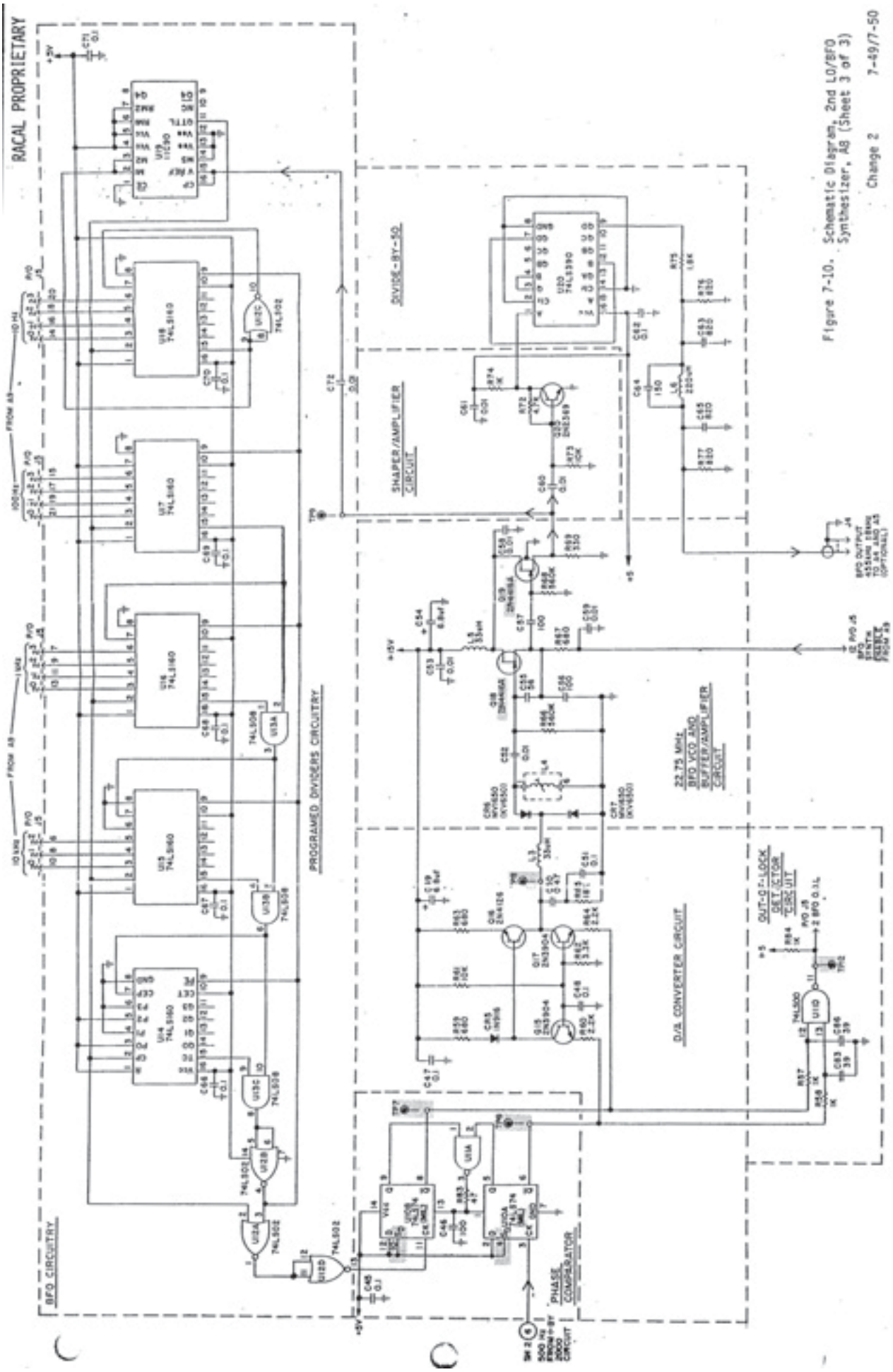

Figure 7-10. Schematic Diagram, 2nd LO/BFO Synthesizer, A8 (Sheet 3 of 3)

Change 2 7-49/7-50

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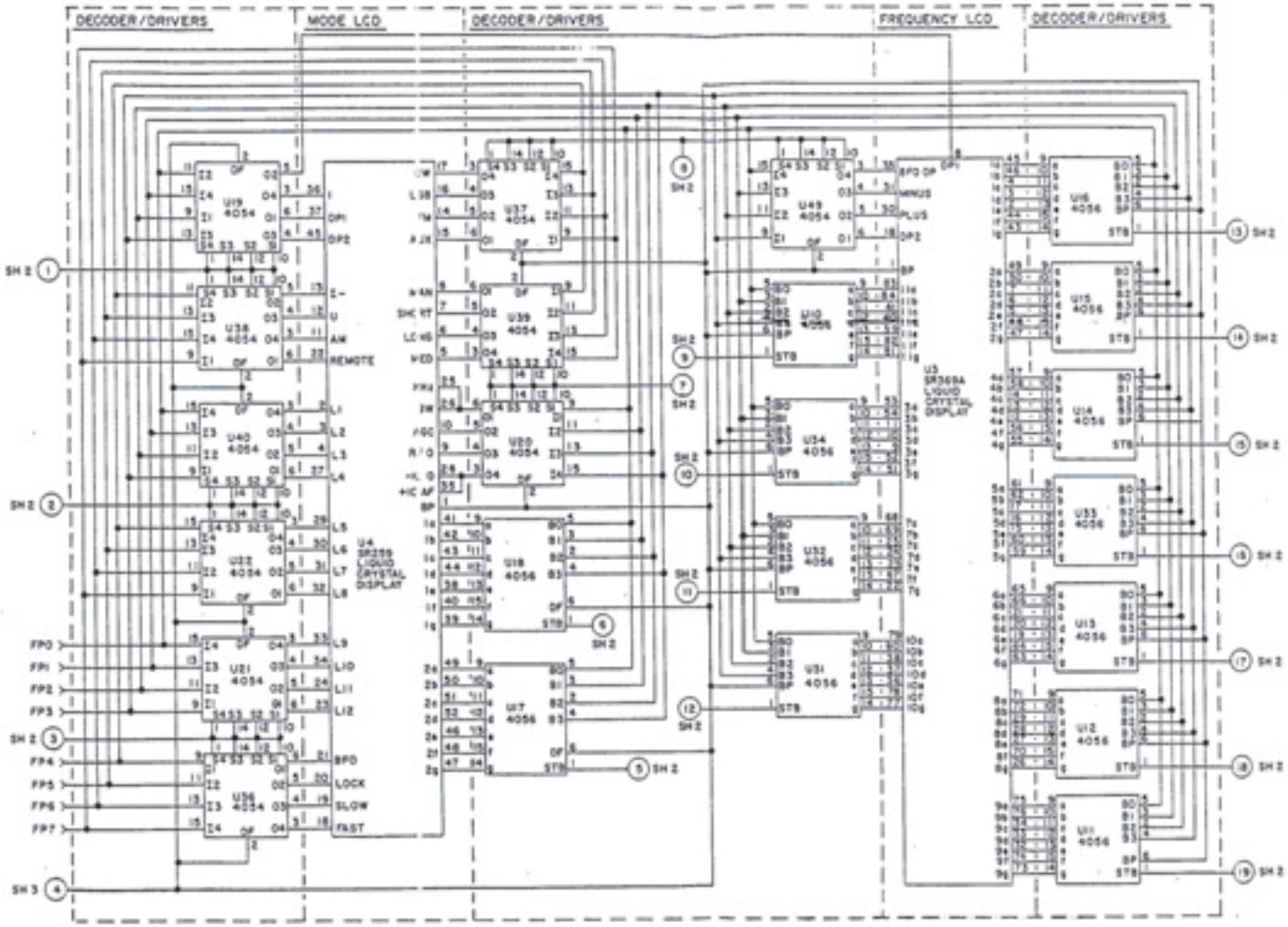

	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23	U32	U33	34	U36	U37	U38	U39	U40	U49
+5	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
GND	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	,8	7,8	7,8	7,8	7,8	7,8	7,8
LOC	G10	A7	C7	D7	G7	J7	K7	D13	E13	K16	D13	F16	G16	C10	D10	F7	10	E16	J13	J16	H13	H16	J10

A	B	A 3
SH 1	SH 2	SH 3
REVISION STATUS OF SHEETS		

Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 1 of 3)

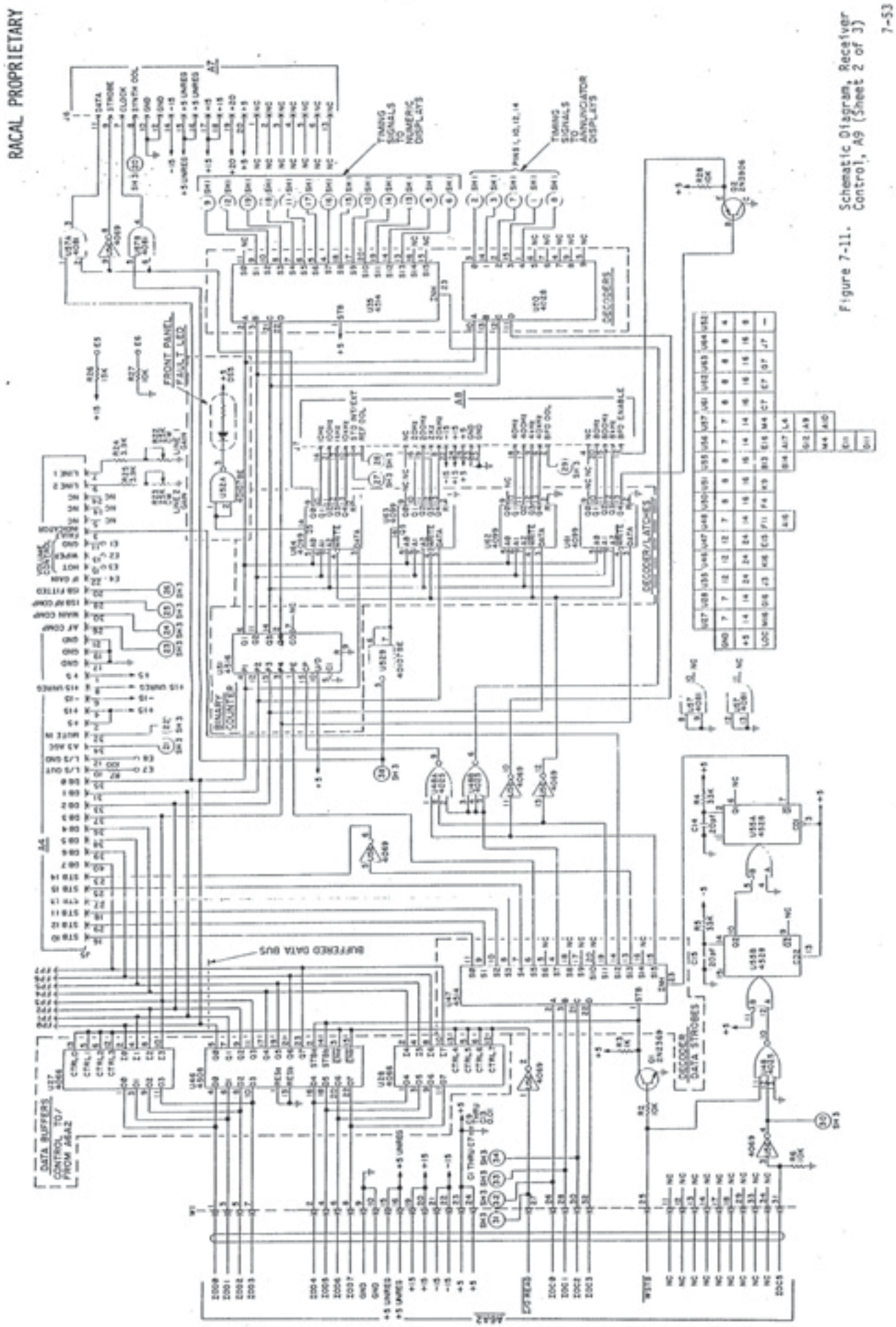

Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 2 of 3)

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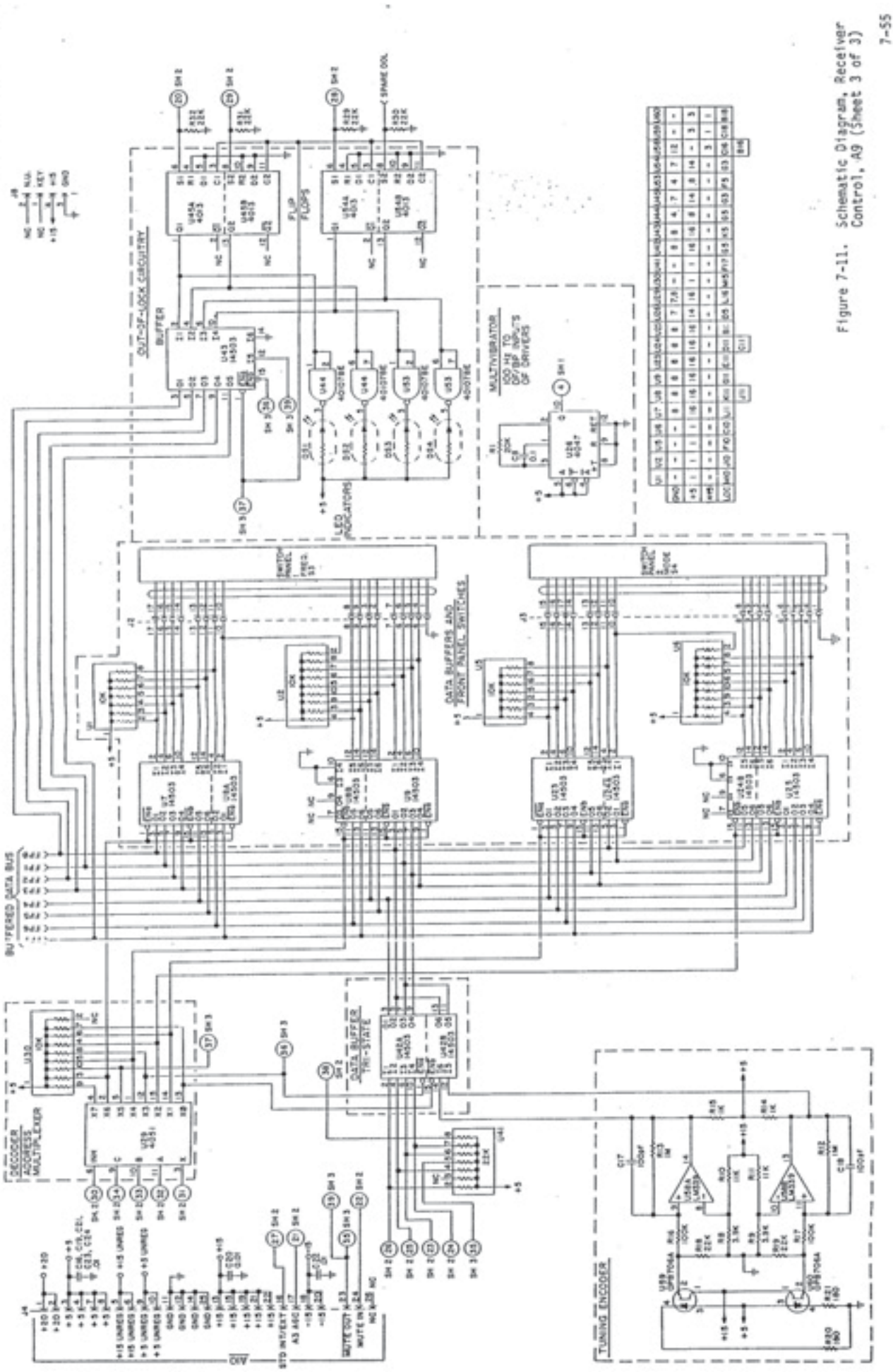

Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 3 of 3)

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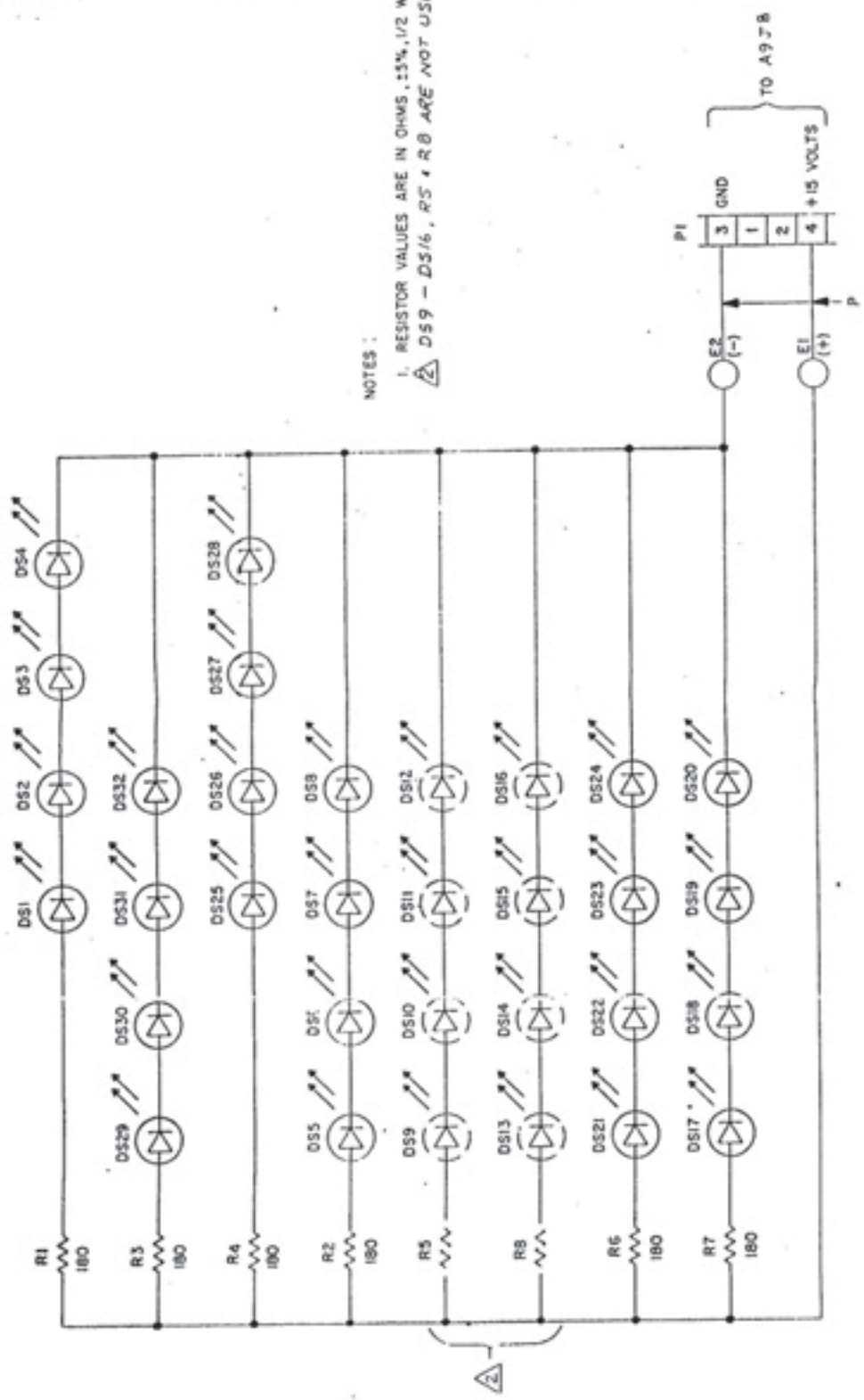

Figure 7-12. Schematic Diagram, Liquid Crystal Display Lamps

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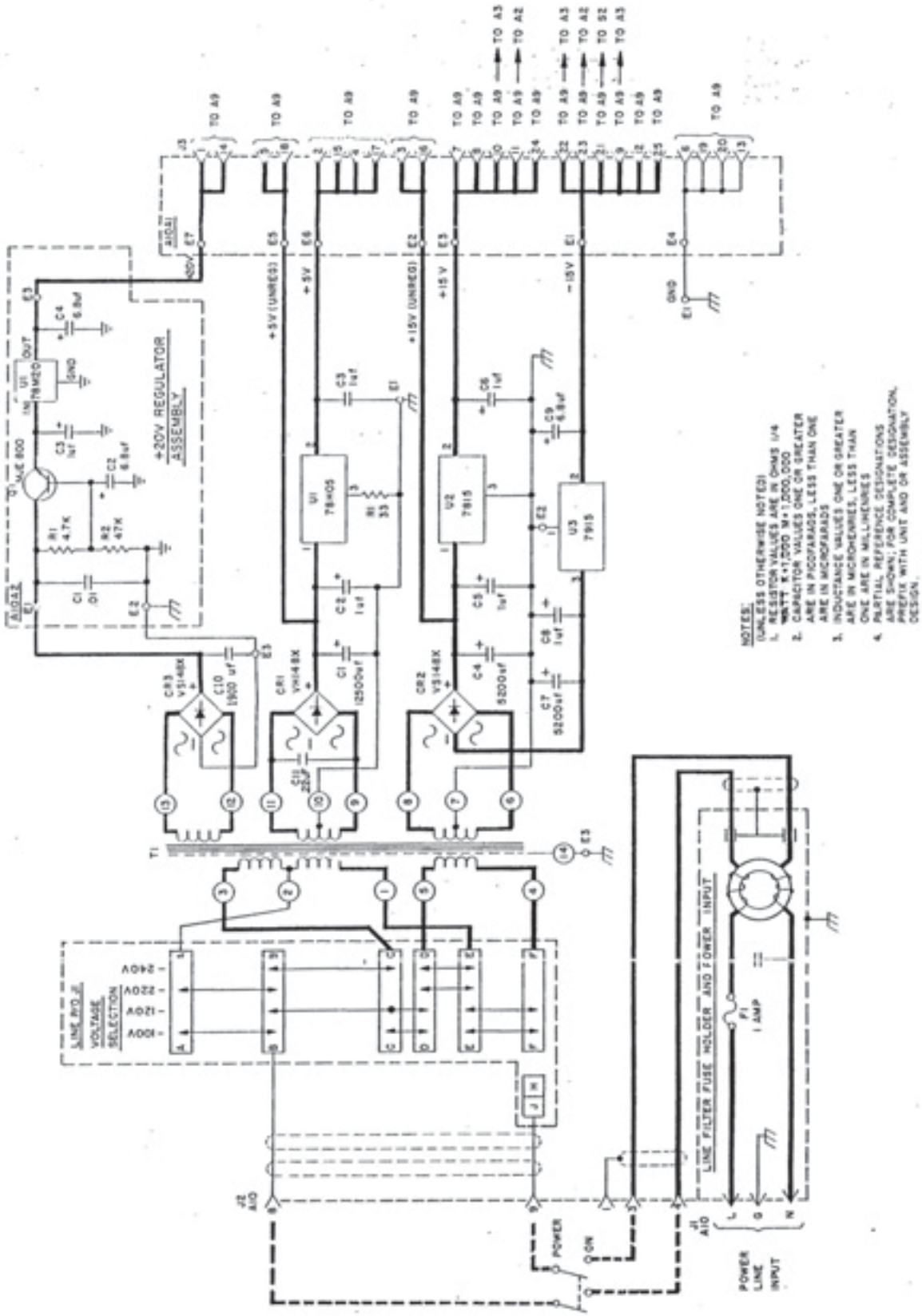

Figure 7-13. Schematic Diagram, Power Supply, A10

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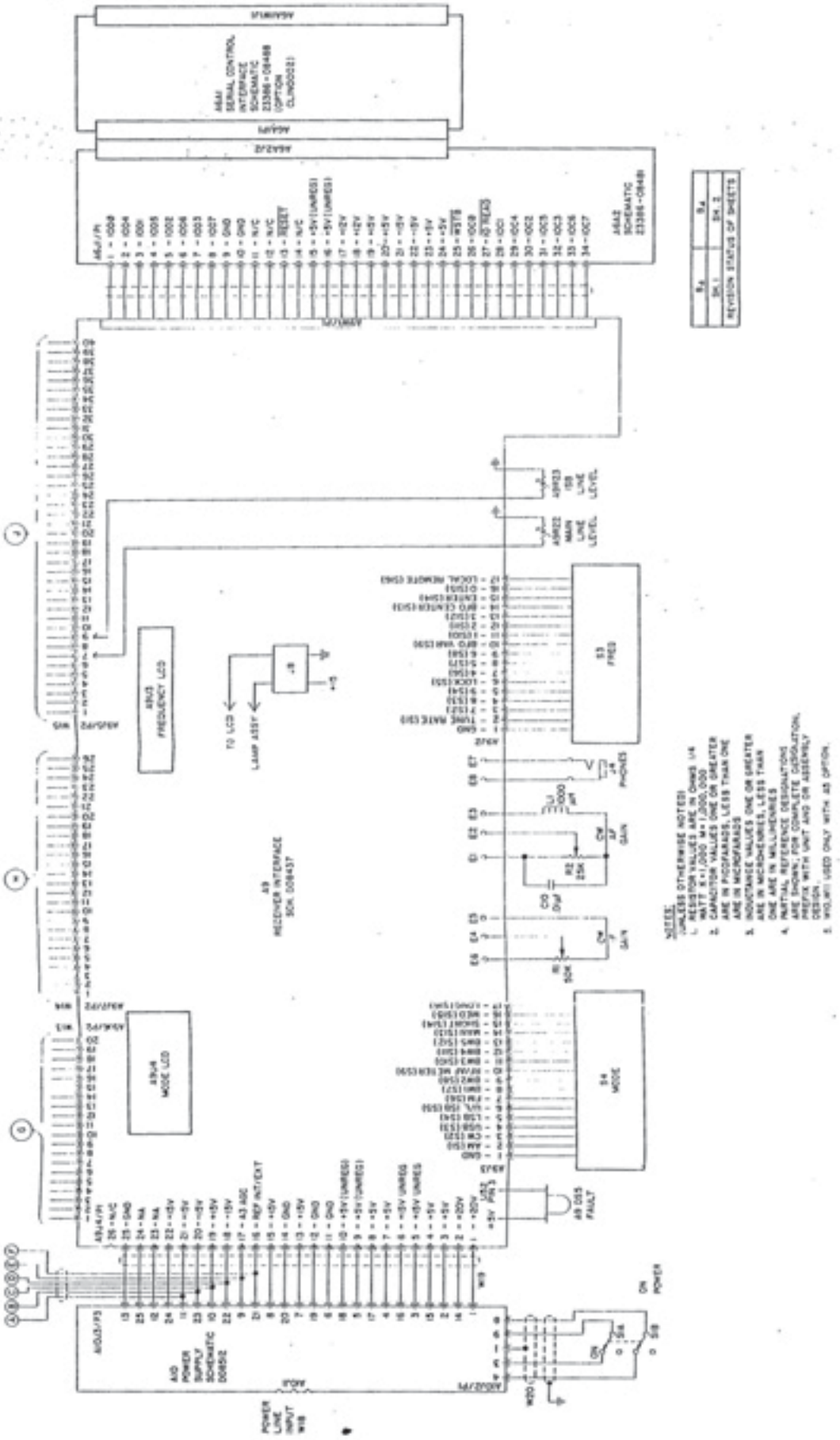

Figure 7-14. Interconnection Diagram, RA6790/GM HF Receiver (Sheet 1 of 2)

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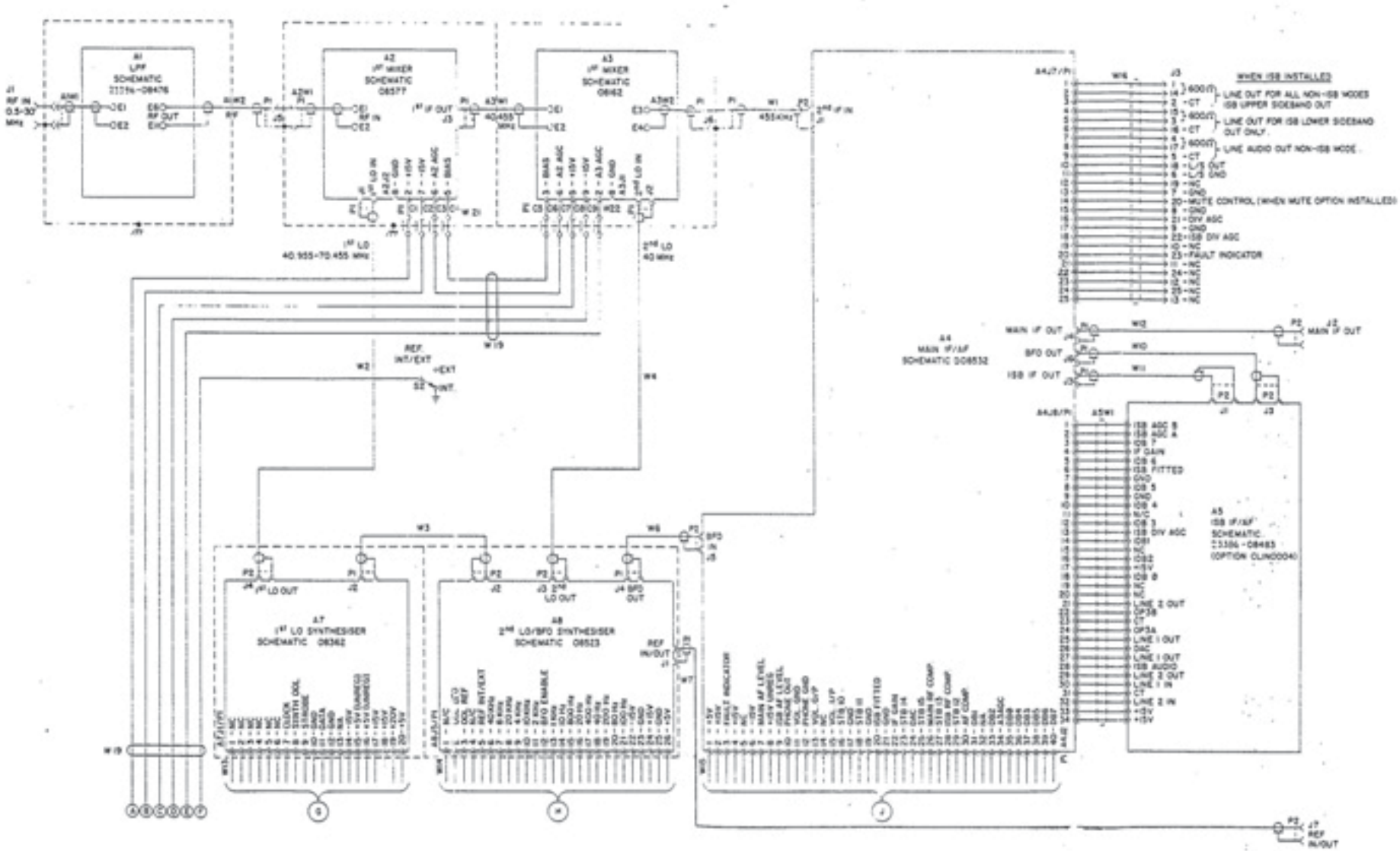

Figure 7-14. Interconnection Diagram, RA6790/GM HF Receiver (Sheet 2 of 2)

SECTION VIII
DIFFERENCE DATA

8.1 **INTRODUCTION**

8.2 The information presented herein identifies the differences between the HF Receiver, Type RA6790/GM (hereinafter referred to as the basic receiver) and the modified receiver, resulting from the addition of an AGC level return software modification.

8.3 **EQUIPMENT MODIFICATIONS**

8.4 Refer to Attachment A "Technical Modification for AGC Level Return" at the rear of this document.

8.5 **SCOPE OF DIFFERENCE DATA**

8.6 In-as-much as the general description, installation, circuit description and maintenance for this manual are not affected by the equipment modifications, the difference data will address only the following. This includes: operation, parts list and schematic diagrams for the microprocessor circuit card assembly (A6A2) within the microcomputer assembly (A6).

8.7 **OPERATION**

8.8 Operation of the modified receiver is identical to that of the basic receiver with the following exception.

8.9 **AGC Level Return** - Refer to paragraph 1-15 in Attachment A.

8.10 **PARTS LIST**

8.11 The information presented herein pertains to usable on code effectivities associated with the modified receiver and provides a listing of replaceable electrical/electronic parts for the microprocessor circuit card assembly (A6A2) within the microcomputer assembly (A6).

8.12. **PARTS LIST DESCRIPTION** - The list of replaceable parts consists of a table which divides the microprocessor circuit card assembly into representative groups of sub-assemblies and components as may be applicable. This subdivision facilitates the identification and requisitioning of replacement parts for the microprocessor circuit card assembly of the modified receiver. It should be noted that the procurement of parts for any sub-assembly/components for the basic receiver, not covered by this parts list addressing the equipment modifications to the modified receiver, may be obtained by referring to Section VI of this manual.

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(Refer to Figure 7-8, Sheet 1, for circuit details)

Figure 8-1. Microprocessor Circuit Card Assembly (A6A2) Schematic Diagram (Sheet 1 of 2)

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(Refer to Figure 7-8, Sheet 1, for circuit details)

Figure 8-1. Microprocessor Circuit Card Assembly (A6A2) Schematic Diagram (Sheet 1 of 2)

8-3/8-4

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(Refer to Figure 7-8, Sheet 2 for circuit details)

Figure 8-1. Microprocessor Circuit Card Assembly (A6A2) Schematic Diagram (Sheet 2 of 2)

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TABLE 8-1. PARTS LIST, MICROPROCESSOR ASSEMBLY, A6A2

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	MFR. PART NO.	USABLE ON CODE
	A6A2	Microprocessor Assembly	08392		
	BT1	Battery, Ni-Cad, 2.4 V dc	42517		
	C1, C2	Capacitor, Ceramic, 15 pF, nonpolarized, ±5%	21351	DTZ-15	
	C3-C10, C18	Capacitor, Ceramic, 0.1 uF, 50 WVDC, ±20%	21732	MS39014101-1593	
	C11, C12	Not Used			
	C13, C14	Capacitor, Tantalum, 6.8 µF, 35 WVDC, ±20%	25060-685	T362A685M035AS	
	C15	Capacitor, Ceramic, 0.001 µF, 50 WVDC, ±20%	21756	CY15C102M	
	C16	Capacitor, Tantalum, 4.7 µF, 10 WVDC, ±2%	25059	T210A475M010MS	
	C17	Capacitor, Tantalum, 15 µF, 20 WVDC, ±20%	25062-156	T362B156K020AS	
	CR1	Diode, Zener, 5.6 V dc	33543	1N752A	
	CR2, CR4, CR5, CR6	Diode, Silicon	35514	1N916B	
	CR3	Diode, Germanium	35538	1N270	
	J1	Connector, 34-Pin	61200		
	J2	Connector, 50-Pin	61224		
	Q1, Q4	Transistor, PNP, Low Power	32037	2N3906	
	Q2, Q3, Q5	Transistor, NPN, Low Power	32036	2N3904	
	Q6, Q7	Transistor, Field Effect	32518	TIS74	
	R1, R7	Resistor, Film, 1 K, ±2%, 1/4 W	12161-102	RL07S102G	
	R2	Resistor, Film, 39 K, ±2%, 1/4 W	12161-393	RL97S393G	
	R3, R8	Resistor, Film, 10 K, ±2% 1/4 W	12161-103	RL07S103G	
	R4, R12	Resistor, Film, 47 K, ±2%, 1/4 W	12161-473	RL07S473G	
	R5	Resistor, 120 K, ±2%, 1/4 W	12161-124	RL07S124G	
	R6	Resistor, Film, 82 K, ±2%, 1/4 W	12161-823	RL07S823G	
	R9	Resistor, 270 ohms, ±2%, 1/4 W	12161-271	RL07S271G	
	R10, R15	Resistor, Film, 33 K, ±2%, 1/4 W	12161-333	RL07S333G	
	R11	Resistor, Film, 47 ohms, ±2%, 1/4 W	12161-470	RL07S470G	
	R13	Resistor, Film, 10 ohms, ±2%, 1/4 W	12161-100	RLR07C100GR	

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TABLE 8-1. PARTS LIST, MICROPROCESSOR ASSEMBLY, A6A2 (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	MFR. PART NO.	USABLE ON CODE
	R14	Resistor, Film, 10 K, ±2%, 1/4 W	12161-104	RL07S104G	
	U1	IC, Central Processor Unit	36710	MK3850	
	U2	IC, System Memory Interface	36712	MK3853	
	U3	IC, Dual 1-of-4 Decoder	36671	M38510/30702BEE	
	U4	IC, Octal 3-State Transceiver	36741	M38510/31004BEA	
	U5, U6, U14	ROM Set, Firmware, RAGM01	A09666		A
	U7, U8	IC, Random Access Memory	36713	PS101L	
	U9	IC, +12 V Regulator, TO-92	36760	LM78L12ACZ	
	U10	IC, Triple 3-Input NAND Gate	36633	M38510/30005BCB	
	U11	IC, Quad 2-Input NOR Gate	36660	MS8510/30301BCB	
	U12	IC, Hex Inverter	36676	M38510/3003BCB	
	U13	IC, Octal D Tri-State F/F	36703	SN74S374N	
	XU5, XU6, XU14	IC Socket, 24 Pin, DIP	76020		
	Y1	Crystal, 2 MHz	08487		
	-	Printed Circuit Card	08482		

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ATTACHMENT A

TECHNICAL MODIFICATION

FOR

AGC LEVEL RETURN

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LIST OF APPENDICES

Appendix	Title
A	Input/Output Electrical Interface
B	Operation with AGC Return Software Installed

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TECHNICAL MODIFICATION
FOR
AGC LEVEL RETURN

1-1. SCOPE

1-2. This document provides technical information on an equipment modification to the HF Receiver, Type RA6790/GM for AGC level return, as well as, addresses the associated circuit changes and receiver deployment, as may be applicable. It should by noted that this modification is a part of the standard configuration for the HF Receiver, Type RA6790/GM.

1-3. INTRODUCTION

1-4. The information presented in the following paragraphs identifies and describes the differences between the HF Receiver, Type RA6790/GM (hereinafter referred to as the standard receiver) and the modified receiver, resulting from an AGC level return software modification to the microcomputer assembly (A6).

1-5. EQUIPMENT MODIFICATIONS

1-6. The standard receiver was modified to provide an AGC level return to all status returns during remote control operation. This level is appended to the status return before a carriage return (CR) in the form Rx. R standing for the AGC return level code and x representing a range from 0 (minimum signal) to 150 (maximum signal). The data character format used for all command and monitor statements during remote control operation, via a remote computer/controller, consists of a start bit, seven data bits, an optional parity bit, and/or two stop bits depending on the optional parity condition. In addition, the AGC return level is sent, via a serial asynchronous RS-232C remote control interface, to the remote computer/controller regardless of AGC mode setting.

1-7. To implement modification to the standard receiver, the existing EPROM set was replaced with a functionally similar circuit, in addition to, being equipped with the necessary software for accommodating AGC level return operation.

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1-8. CIRCUIT CHANGES

1-9. The following paragraphs describe those circuits that were replaced and/or changed to implement the equipment modifications.

1-10. MICROCOMPUTER ASSEMBLY (A6) - The microcomputer assembly consists of two separate circuit card assemblies. These include: the serial asynchronous interface (A6A1) and the microprocessor (A6A2) circuit card assemblies. However, for this application only the microprocessor circuit card assembly (A6A2) is to be considered. The microprocessor circuit card assembly used in the modified receiver is physically and functionally the same as the assembly used in the standard receiver with the following exception. The integrated circuits U5, U6, U14 firmware EPROM, ROM set, part number 08449 was replaced with an EPROM, ROM set, Type RAGM01, part number A09666, as a result of the software modification to implement AGC level return operation. In addition, this software modification also provides the modified receiver with a low frequency reception extension to 50 kHz, however, with degradated response below 500 kHz.

1-11. RECEIVER DEPLOYMENT

1-12. The following paragraphs address the installation, operation and maintenance of the modified receiver.

1-13. INSTALLATION - The physical installation of the modified and standard receivers is identical. However, refer to Appendix A for additional technical information concerning the input/output electrical interface for implementing remote control operation, as appropriate.

1-14. OPERATION - Operation of the modified receiver is identical to that of the standard receiver with the following exception.

1-15. AGC Level Return - During remote control operation, the modified receiver will append an AGC level to all status returns in the range of 0-150 (minimum to maximum signal), using a standard ASCII data character of the form Rx. Refer to Appendix B for technical information concerning local and remote operation, as appropriate.

1-16. MAINTENANCE - Maintenance of the modified receiver is the same as for the standard receiver.

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APPENDIX A

INPUT/OUTPUT ELECTRICAL INTERFACE

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APPENDIX A

INPUT/OUTPUT ELECTRICAL INTERFACE

A-1. INTRODUCTION

A-2. The digital input output connector type is M83723-02R-1626N.

The receiver address, baud rate, and parity option may be selected by grounding pins on the input output connector. See Figure A-1.

Separate lines are provided for command input and monitor output data.

The command receiver meets the specifications of RS423 and MIL-STD-188-114. It is interoperable with MIL-STD-188C or RS232 compatible devices. In addition, the command receiver is interoperable with MIL-STD-188C or RS232 compatible devices.

The monitor transmitter meets the specifications of RS423 and MIL-STD-188-114. It is interoperable with MIL-STD-188C or RS232 compatible devices. In addition, the interface may be strapped for RS422 unipolar operation.

The interface allows up to ten receivers to be placed on a common parallel input/output bus.

The data character is the standard ASCII asynchronous format consisting of one start bit, seven data bits (one ASCII character), one optional parity bit, and one of two stop bits depending on parity condition. See Figure A-4.

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PIN	FUNCTION
A	System Ground
B	Data Out A
C	Data Out Ground
D	Data Out B
E	Ground
F	Data in A'
G	Data in Ground
H	Ground in B'
J	Ground
K	Receiver # D1-1
L	Receiver # D1-2
M	Receiver # D1-4
N	Receiver # D1-8
P	Receiver # D2-1
R	Receiver # D2-2
S	Receiver # D2-4
T	Receiver # D2-8
U	/ Parity Select
V	Parity Even / Odd
W	Baud Rate B4
X	Baud Rate B3
Y	Baud Rate B2
Z	Buad Rate B1
a	Ground
b	Ground
c	System Ground

NOTES:

1. Data Input/Output "A" - Mark is negative.
2. Data Input/Output "B" - Mark is positive.
3. For unipolar ballanced (RS-422) operation, a jumper may be changed on the board.
4. The address, Parity option, and Baud rate are configured as follows:
   Logic 1 - Open Circuit
   Logic 0 - Ground
5. The Baud rate selection is shown in Figure 2.
6. The data transmitters and receivers may be wired as shown in Figure 3.

Figure A-1. Digital Interface Connector A6A1 Pin Assignment

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CODE (HEX)	BAUD RATE
0	50
1	75
2	110
3	134.5
4	150
5	300
6	600
7	1.2k
8	1.8k
9	2k
A	2.4k
B	3.6k
C	4.8k
D	7.2k
E	9.6k
F	19.2k

Figure A-2. Baud Rate Selection

A. RS423, RS232, MIL-STD-188-114 Unbalanced

A6A1J1	A	System Ground
	B	Data Out (a)
	C	Data Out Ground
	D	
	E	
	F	Data In (a')
	G	Data In Ground
	H	
	J	

B. RS422

A6A1J1	A	System Ground
	B	
	C	Data Out (a)
	D	Data Out (b)
	E	
	F	Data In (a')
	G	
	H	Data In (b')
	J	

Figure A-3. Interface Wiring For Various Control Systems

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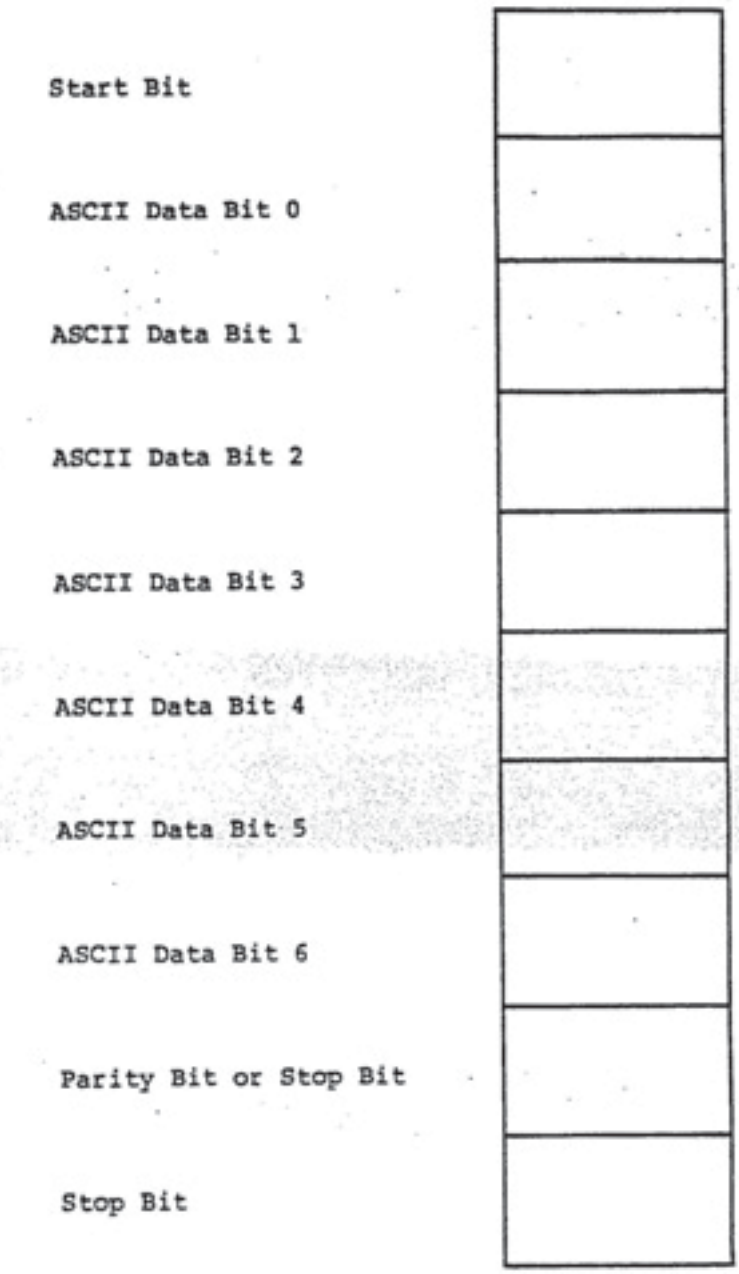

Figure A-4. Data Character Format

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APPENDIX B

OPERATION WITH AGC RETURN SOFTWARE INSTALLED

B-1. LOCAL OPERATION

B-2. Operator front panel control is described for selection of frequency, BFO offset, detector mode, AGC time constant, and bandwidth. Also the operator may select audio or RF signal strength indications on the meter, adjust audio and RF gain, and select local or remote control operation. In addition, secondary pushbutton control allows the operator to invoke the build in test function (BITE) and to manually force the filter complement display to any desired set-up.

a. Frequency Selection: The receiver operating frequency may be set in two ways: First, gross changes in frequency may be made rapidly via the push-buttons. Depress the ENTER key, then input the desired frequency using the digit pushbuttons 0-9. The new freqeuncy will be displayed on the LCD panel, starting at the left-most, 10 MHz digit, and progressing to the right. The second method of frequency selection involves the tuning wheel. The tuning wheel is enabled to enter frequency whenever the tune select pushbutton has been depressed, selecting FINE (1 Hz increments), SLOW (30 Hz increments) and FAST (100 Hz increments). (Note that FINE does not display on the auxiliary LCD panel, but SLOW and FAST do.) For protection, LOCK may be selected, disabling the tuning wheel from all functions, so the operating frequency may not be changed inadvertently. Rotating the wheel clockwise will increase the frequency, counterclockwise will decrease the frequency, in the increments chosen.

b. BFO Selection: For CW reception, set the BFO to the required offset frequency by selecting the BFO tuning function and spinning the tuning wheel until the desired BFO offset is displayed. (LOCK will also protect the BFO setup, if depressed.) Depressing the BFO/CENTER button will center the BFO at the IF for use as a zero beat tuning aid. Depressing this button again will restore the original chosen offset frequency. The BFO may not be tuned in the BFO center mode. This BFO center mode is indicated by the display in the BFO frequency of only the first digit and decimal point.

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c. IF Bandwidth: Select the desired IF bandwidth by depressing BW1 through BW5. BW1 will select the narrowest IF filter installed. Increasing BW numbered buttons will select increasing filter bandwidths.

d. Detection Mode: AM, FM, CW or separate SSB detection modes may be selected by depressing the appropriate pushbutton. ISB mode for receivers so equipped, may be activated by depressing the ISB pushbutton. Pressing this button will activate both USB and LSB reception channels simultaneously, and will connect the headphone to the last monitored ISB channel, subsequent depressions of the ISB button will connect the headphone to the LSB or USB channels as indicated by the LCD display.

e. AGC Time Constant selection is made via the SHORT, MEDIUM, and LONG pushbuttons. In addition, a variable threshold gain control mode is available which uses manual gain in conjunction with AGC so that a signal below the AGC threshold point, as determined by the IF gain control is cut off while a signal above the MGC threshold is captured by AGC. This is selected using the above switches in conjunction with the MGC button.

f. Manual Gain Control (MGC) or Variable Threshold gain control of the receiver IF strip is enabled by use of the MGC button. The receiver IF strip gain is then controlled by the IF gain control on the front panel, or the minimum set by the IF gain control in variable threshold mode.

g. Audio level to the headphones is set by the AF GAIN control. Audio to the line output is determined by the MAIN LEVEL audio control and indicated by the LCD meter when AF is selected on the meter. Audio to the line output for ISB-LSB is determined by the preset ISB-L control on the front panel, if ISB is installed. If it is installed, the ISB-U line output is set by the main level control, and the main AF output is now switched between upper and lower sideband as determined from the front panel.

h. Meter Selection, AF or RF, is controlled via the METER RF/AF button.

i. Remote/Local control of the receiver is selected by alternate depression of the REMOTE/LOCAL pushbutton.

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j. BITE, or the built in test function, can be invoked in local mode at any time by simultaneously depressing LOCK and AM. BITE will then determine, organize, and display the bandwidths of the IF filters installed in the receiver, as well as test receiver parameters for proper operation. Any errors will be displayed on the main LCD display. (See Table B-2 for list and explanation of errors.) If there are no errors, the receiver will return to its pre-BITE frequency, detector mode, etc., when BITE is complete, and will use and display the new filters data. If any errors were encountered, the old filter data will remain unchanged. In addition:

LOCK and CW can be used to force BITE to proceed to the next sequential test after an error has caused it to stop.

LOCK and USB can be used to force BITE to cycle in a tight scope loop for analysis

LOCK and LSB can be used to prematurely terminate BITE.

k. Forced Bandwidth Setup is accomplished, in case BITE results are unsatisfactory, by simultaneously depressing LOCK and ISB (but not during BITE!) The LCD display will indicate AUX. Entry of symmetrical filters is accomplished using the digits 0-9, in 100 Hz steps, delimited with the ENTER key. For example, to enter a .4 kHz (400 Hz) filter, "4" and "ENTER" would be pressed. To enter 20 kHz, "2", "0", "0", "ENTER" would be pressed. (200 x 100 Hz = 20 kHz). USB and LSB filters can be loaded also, using the USB and LSB pushbuttons, each time followed by ENTER. Blank filter slots can be loaded simply by pressing the enter key again. When all seven filter slots have been loaded, the AUX indicator will go off automatically, disabling any further changes, and resetting the receiver to normal operation. If it is desired to terminate this function before all slots have been changed it is only necessary to depress ISB.

B-3. REMOTE OPERATION

B-4. See Table B-1 for a complete list of remote commands and usage. The data is coded as ASCII characters, and transmitted as a string terminated with a carriage return. A typical string would look like the following:

F2.35D3I1.2M4B-2.3A37(CR)

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The Carriage Return (CR) is the trigger to the receiver to set up the data from all commands received since the last carriage return. All monitor data streams are terminated with a carriage return.

Table B-1. Command and Monitor Data and Format

A. Receiver Number ($85)

The ASCII followed by two optional numeric characters shall select the receivers to respond to this and all subsequent commands, until changed by another "$" command.

The "$" character followed by no numbers is a system wide unlisten command. Multiple receivers may be addressed with one command sequence by separating the receiver numbers with commas. Multiple addressing may not be used to set control modes or to specify a talker.

B. Frequency (F3.415926)

The main tune Frequency is entered in MHz in up to eight digits with optional decimal point. Leading and trailing zeros may be removed from the command. The frequency given is the true carrier frequency except for the sideband detection modes, when the frequency is that of the virtual carrier.

C. Detector (D3)

The detection mode of receiver is set with this command. The modal commands are:

1 - Amplitude Modulation
2 - Frequency Modulation
3 - Continuous Wave, Variable Offset
4 - Continuous Wave, Center Tuned
5 - Independent Sideband (I-LSB AGC Meter Level Returned)
6 - Lower Sideband
7 - Upper Sideband
8 - Independent Sideband (I-USB AGC Meter Level Returned) See Paragraph L.

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Table B-1. Command and Monitor Data and Format (Cont.)

The detection mode contains four non-modal override commands which may be used for maintenance and test purposes. These commands are distinguished from the modal commands by the "=" placed between the letter and the command number. (D=1).

=1 - Envelope Detector
=2 - Continuous Wave Detector
=3 - Frequency Modulation Detector
=4 - ISB

When an override command is given here it must also be used to select the IF filter.

D. IF Bandwidth (I6)

The IF Bandwidth is specified in kiloherz. The receiver selects the bandwidth closest to the one requested. The monitor data shows the actual bandwidth picked.

In override mode the command becomes I=3, where the number is the filter slot number from one to seven. When in ISB override mode, the I= command must be used to select the USB filter.

E. AGC Mode (M2)

The AGC mode and rate are specified as follows:

1 - Short AGC time constant
2 - Medium AGC time constant
3 - Long AGC time constant
4 - Manual IF attenuation
5 - Short time constant Variable Threshold mode
6 - Medium time constant Variable Threshold mode
7 - Long time constant Variable Threshold mode

F. BFO Frequency (B-1.82)

The BFO offset from center frequency, specified in kHz is entered with this command. The data is used in the modal system in CW only.

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Table B-1. Command and Monitor Data and Format (Cont.)

G. Attenuation (A30)

The attenuation number defines the amount of attenuation placed in the signal path during the manual attenuation AGC mode, or the minimum attenuation during the variable threshold modes. The attenuation varies from zero (no attenuation) to 150 (maximum attenuation) with no change between numbers greater than 3 dB.

H. Status (S5)

The status command when sent to the receiver controls its operating status. In the monitor mode the status provides summary error indication.

1) Command Status

Command status may only be sent to one receiver, since commands 5 and 6 create monitor data streams. The status commands are:

1 - Set the receiver to local control.
2 - Set the receiver to remote control.
3 - Execute the BITE self test routine.
4 - Terminate the BITE self test routine.
5 - Report currently installed bandwidths.
6 - Report BITE results.
7 - Force bandwidth setup.
8 - Enable remote AGC dump.
9 - Inhibit remote AGC dump.

Command 1 - Sets the receiver to local control mode. This command is invalid in override mode.

Command 2 - Sets the receiver to the remote control.

Command 3 - Starts receiver Bite (Built in Test) routine.
This command, when excepted causes the receiver to output a colon (:) until bite is finished it will output a colon response to any talk command.

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Table B-1. Command and Monitor Data and Format (Cont.)

Command 4 - Terminate Bite - causes the receiver to assume its pre Bite status.

Command 5 - Report current bandwidths. This command causes the receiver to list the installed filter bandwidths in slot number order followed by a carriage return.

(FL1), (FL2), (FL3), (FL4), (FL5), (FL6), (FL7), (CR)

A typical output might be L,, 6.2, U, .4, 20, (CR)
Which reports the following:

Slot	Filter Modification
1	Lower Sideband Filter
2	Nothing
3	1.2 kHz Symmetric Filter
4	Upper Sideband Filter
5	400 Hz filter
6	20 kHz filter
7	Nothing

Command 6 - Report results of last bite. Note that this is not cleared after having been read, nor does it cause another Bite cycle. To get a new Bite cycle with report, start with S3, then go to S6.

GOOD response - OK XX (CR)
BAD response - 4, 17, 33 End XX (CR)

Command 7 - Force Receiver Bandwidth setup.

This command is used to force a particular filter complement in the GM receiver. Allowable codes are L for Lower Sideband, U for Upper Sideband, N for None, and bandwidths up to 20 kHz in kHz with a resolution of 100 Hz. Symmetric bandwidths in kHz are terminated with a comma.

The string may contain all seven filters or it may end early with a (CR). Slots not entered will not be altered by the S7 command.

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Table B-1. Command and Monitor Data and Format (Cont.)

The command:

Slot	Filter Modification
1	Lower Sideband Filter
2	Upper Sideband
3	1.7 kHz Symmetric
4	400 Hz Symmetric
5	Unused
6	3.2 kHz Symmetric
7	Unchanged from previous setting

Command 8 - Enable AGC Dump

This command causes all subsequent commands containing receiver data to cause an automatic AGC dump.

Command 9 - Inhibit AGC Dump

This command causes the AGC command dump to be disabled. This would be used when free tuning the receiver by remote control.

2) Monitor Status

The following summary status is appended to all other monitor data streams:

1 - Receiver operating in remote control
2 - Synthesizer out of lock
4 - Receiver in Override remote control mode
8 - Last command sequence had character transmission error
16 - Last command sequence had data error
32 - Lost data error in last sequence

The indicators above are added together to from the summary status. For instance 17 indicates remote operation with a data error in the last command stream.

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Table B-1. Command and Monitor Data and Format (Cont.)

I. Monitor Command G (G)

This command is the overall monitor command. All data relevant to the current status is returned on receipt of the trigger.

J. Monitor Command T (TFI)

This is the selective monitor command. It allows the controller to specify the data to be returned in the monitor data stream generated following the carriage return trigger.

The monitor commands will be ignored unless sent to only one receiver.

The selective monitor command must immediately precede the carriage return to avoid confusion with the data commands which use the same letter control characters.

K. Override Mode Notes.

The override mode gives the remote controller functional level control of the receiver. That is, the first local oscillator is always tuned to 40.455 MHz above the entered frequency. The IF slot is always enabled regardless of the type of filter installed. It is up to the controller to decide what the filter should be used for, the type of detection mode to employ, and the BFO offset to receive a signal. For instance, in sideband detection with a symmetrical filter, the first local oscillator and BFO must be properly offset to correctly demodulate the signal. The controller also assumes the responsiblity for ensuring that the filter is installed in the selected slot, since an empty slot will cause a dead receiver.

The override mode blanks the display. In addition, override signals cannot be handed off to the operator, since the machine has no way of deciding the difference between a sideband signal with virtual carrier offset or a CW signal with a copy BFO offset. Consequently status command S1 is invalid in override mode.

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Table B-1. Command and Monitor Data and Format (Cont.)

The override mode is invoked when both detector and bandwidth are sent in the same command with the = sign. Sending either without the equals stores the = data but leaves the receiver in the modal command mode.

L. AGC Level Return (R30).

This number is appended to all Status returns and is in the range 0 (Minimum Signal) to 150 (Maximum Signal). It is sent to the remote controller regardless of the AGC mode setting, i.e., whether in MAN, SHORT or any combination of the same.

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Table B-2. Bite Error Table

ERROR NUMBER	DESCRIPTION
1	First Local oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.
2	Second Local Oscillator (reference) synthesizer not locked.
3	First Local Oscillator synthesizer does not break lock to enter fast sampling mode on 500 kHz step change.
4	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.
5	First and Third Local Oscillator synthesizers not locked after 100 millisecond delay from 500 kHz and 500 Hz step change, respectively.
6	Filter slot one contains a symmetrical filter, but there are SSB filters also in the system.
7	Filter slot one contains an upper sideband filter. ISB operation, if installed, will be impaired.
8	No USB filter has been found in the system, and filter slot one does not contain a Symmetrical filter.
9	Not used.
10	Not used.
11	No LSB filter has been found in the system and filter slot one does not contain a symmetrical filter.
12	No symmetrical filters have been found in the system.
13	Filter slot one does not contain a lower sideband filter, but ISB is installed.
14	Random access memory test Failure: Data written to memory different from data read back.
15	Either no filters are installed in the system, or the synthesizer signal strength is out of range prescribed for BITE.
16	Filter slot one contains no filter.
17	Two or more LSB filters have been found in the system.

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Table B-2. Bite Error Table (Cont.)

ERROR NUMBER	DESCRIPTION
18	Two or more USB filters have been found in the system.
19	Although a lower sideband filter has been found in the system, it is not installed in filter slot one. ISB operation, if installed, will be impaired.
20	Not used.
21	Filter in filter slot one is skewed from the IF center frequency.
22	Filter in filter slot two is skewed from the IF center frequency.
23	Filter in filter slot three is skewed from the IF center frequency.
24	Filter in filter slot four is skewed from the IF center frequency.
25	Filter in filter slot five is skewed from the IF center frequency.
26	Filter in filter slot six is skewed from the IF center frequency.
27	Filter in filter slot seven is skewed from the IF center frequency.
28	Not used.
29	Not used
30	Not used
31	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot one.
32	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot two.
33	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot three.
34	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot four.

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Table B-2. Bite Error Table (Cont.)

ERROR NUMBER	DESCRIPTION
35	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot five.
36	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot six.
37	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot seven.

B-13/B-14 blank

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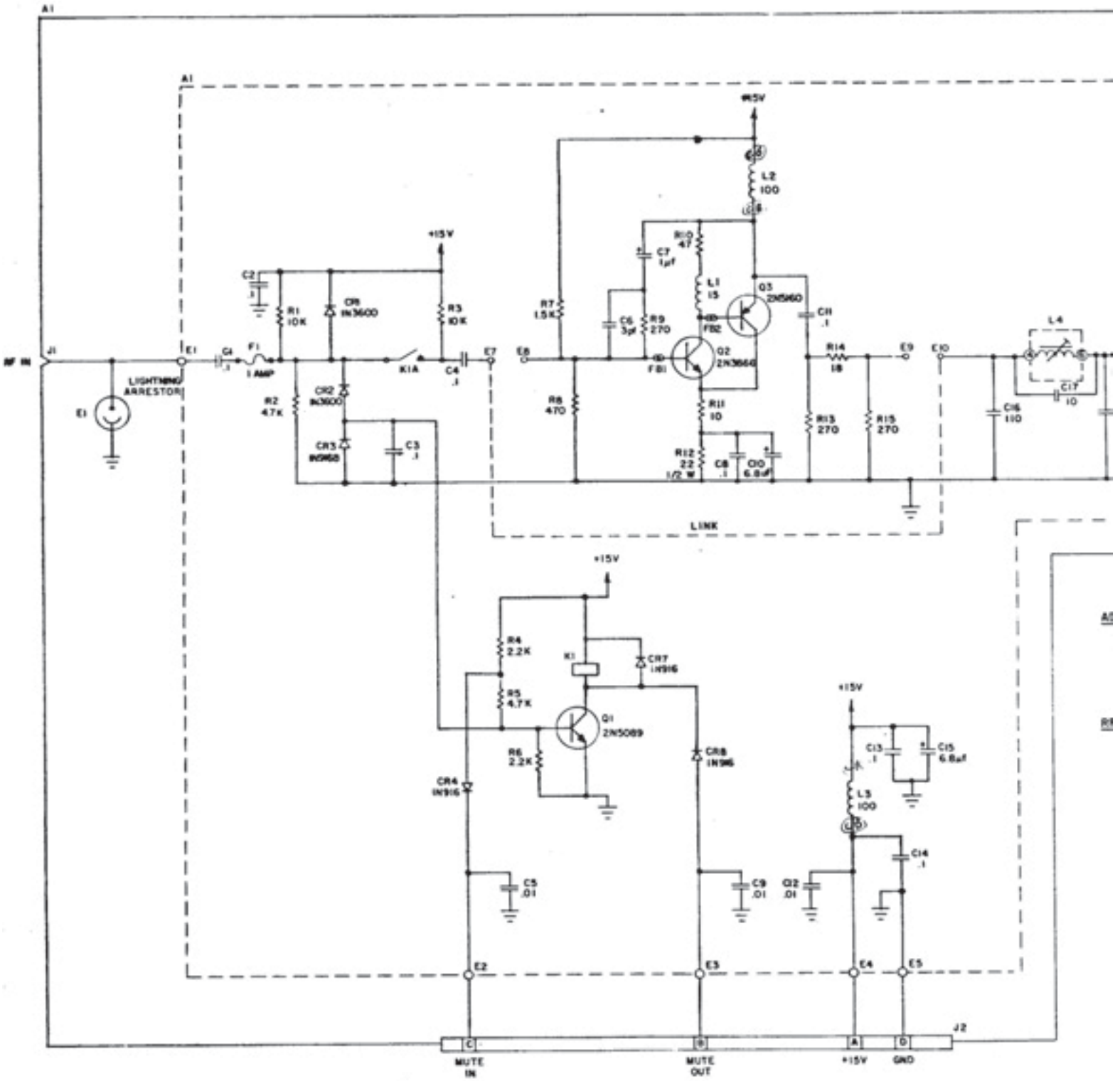

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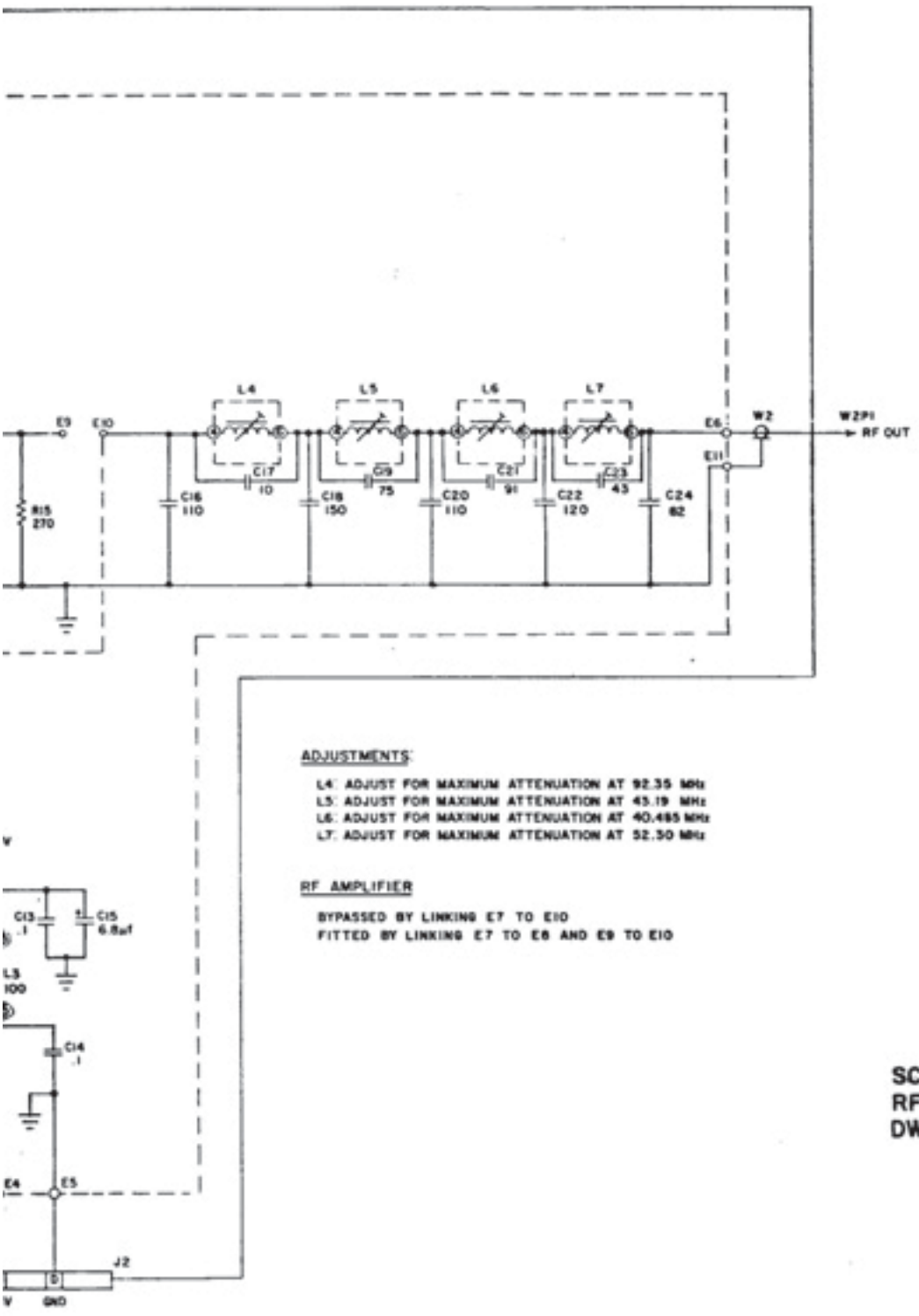
RF STAGE GAIN =

7-10 DB



ADJUSTMENTS:

L4: ADJUST FOR MAXIMUM ATTENUATION AT 92.35 MHz
L5: ADJUST FOR MAXIMUM ATTENUATION AT 45.19 MHz
L6: ADJUST FOR MAXIMUM ATTENUATION AT 40.485 MHz
L7: ADJUST FOR MAXIMUM ATTENUATION AT 52.50 MHz

RF AMPLIFIER

BYPASSED BY LINKING E7 TO E10
FITTED BY LINKING E7 TO E8 AND E9 TO E10

UNLESS OTHERWISE NOTED

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.

SCHEMATIC
RF AMP/LPF MODULE
DWG. NO. D08075

Figure B-3. RF/LPF Module A1 Schemati

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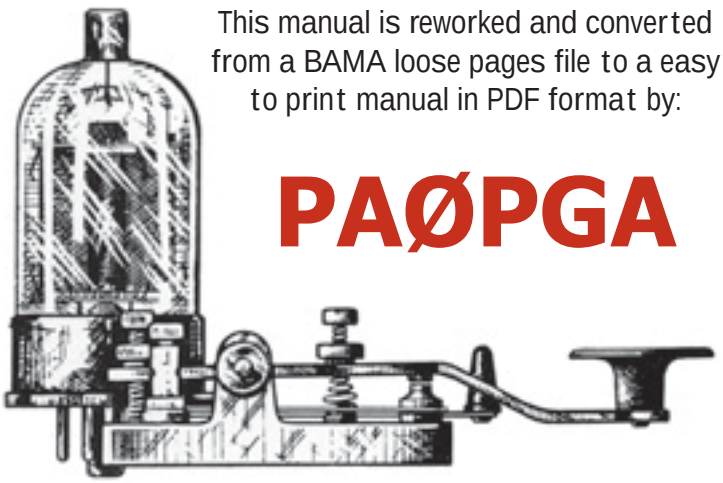

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